SURFACE ENGINEERING FOR SILICON CARBIDE INTERFACE

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A thesis submitted to the Faculty of Science, Agriculture and Engineering

for the degree of Doctor of Philosophy

NEWCASTLE UNIVERSITY

SCHOOL OF ENGINEERING

JUNE 2018

To

my beloved wife

children

abah and mak

ACKNOWLEDGEMENTS

The author would like to express my gratitude to those who had extended their help and support throughout my studies; towards the completion of this thesis in particular.

My thanks and gratitude goes to my supervisors, Dr. Alton Horsfall, Prof Nick Wright and Dr Ming who were always there, providing guidance, support and motivation throughout my study. I would also like to thank Dr. Konstantin for his kindness in helping with the clean room works.

I am thankful to my colleagues, Chloe Peaker, Oras Al-Ani, Fatimah Bahrani, Hind Alsnani, Hua Khee Chan, Faiz Arith, Syazwina Mohamed, Tiago Marinheiro, Luke Bradley, Johan Gausden, Enrique Escobedo-Cousin, Sami Ramadan, Srinivas Ganti, Hector Oyem, Andres Aldana, Paolo Comaron and many more who have contributed and make my years in pursuing PhD interesting as it is challenging.

I am grateful for the services provided by INEX for the deposition of SiO_2 and Dr. Isabel Arce Garcia at NACMA for the SEM imaging. I am indebted to both Universiti Teknikal Malaysia Melaka and the the Ministry of Higher Education (MOHE) for sponsoring my study through the SLAB scholarship.

My special thanks to my wife Nurhidayu, my children Izz Haikal and Izz Haidar for their great patience and support. Not to be forgotten, my parents and other family members for their continuous moral support.

ABSTRACT

Silicon carbide technology has made a significant improvements in these recent years, with a range of different devices, such as diodes, junction field effect transistors (JFETs) and metal-oxide-semiconductor field effect transistors (MOSFETs) becoming commercially viable. The availability of relatively large and high quality wafers of 4H-SiC for device development has facilitated exciting breakthroughs throughout the world. The application areas of 4H-SiC devices include extreme environments such as high power, high frequency, high temperatures as well as optoelectronics. SiC technology has became indispensable due to the increasing demands from industrial sectors including automotive, military and aerospace. One of the crucial challenges for 4H-SiC MOSFETs is to increase the channel mobility which is plagued by the high density of interface traps. Post oxidation annealing (POA) in nitrogen gas environment or nitridation has become a standard process for the fabrication of MOSFETs with acceptable channel mobility around 35 cm^2/Vs, only about 4 $\%$ of the bulk mobility. POA using phosphoryl chloride ($POCl_3$) or phosphorus pentoxide (P_2O_5) sources converts SiO_2 into phospho-silicate glass (PSG) and has succesfully improved the channel mobility by a factor of 3 in comparison to nitridation. However, PSG is a polar material that increases the instability of MOS devices characteristic especially at high temperatures.

In this work, the effect of inclusion of phosphorus (at an atomic concentration below 1 $\%$) on the high temperature characteristics (up to 300°C) of the SiO_2/SiC interface is investigated. Capacitance – voltage measurements taken over a range of frequencies have been utilized to extract parameters including flatband voltage, threshold voltage, effective oxide charge, and interface state density. The variation of these parameters with temperature has been investigated for bias sweeps in opposing directions and a comparison made between phosphorus doped and undoped oxides. At room temperature, the effective oxide charge for SiO_2 may be reduced by the phosphorus termination of dangling bonds at the interface. However, at high temperatures, the effective charge in the phosphorus doped oxide remains unstable and effects such as flatband voltage shift and threshold voltage shift dominate the characteristics. The instability in these characteristics was found to result from the trapped charges in the oxide ($\pm 10^{12}$ cm^{-3}) or near interface traps at the interface of the gate oxide and the semiconductor (10^{12} to $10^{13} cm^{-2}$ eV^{-1}). Hence, the performance enhancements observed for phosphorus doped oxides are not realised in devices operated at elevated temperatures.

The electrical characteristics of 4H-SiC CMOS capacitor and transistor structures have been compared to the recently developed inversion MOS capacitor structure. Parameters including the interface state density, flatband voltage, threshold voltage and effective charge have been acquired from C-V characteristics of MOS capacitors to assess the effectiveness of the fabrication process in realising high quality gate dielectrics for CMOS process. A maximum critical electric field, in excess of 9.5 MV/cm has been demonstrated by the MOS capacitors without sustaining any oxide breakdown. Whilst, the interface trap density extracted from the n-type MOS capacitor is strongly correlated with n-channel field effect mobility, the channel mobility in the p-channel data shows no correlation. The impact of elevated temperatures on device characteristics of MOS capacitors and MOSFETs were also investigated utilizing C-V and I-V measurements performed at temperatures up to 400 °C. The temperature dependence of the flatband voltage, effective oxide charge and interface state density for MOS capacitors and the field effect mobility, threshold voltage and substhreshold swing for MOSFETs was examined in this section to study the effect of different dielectric formation at elevated temperatures. Finally, for the first time, the characteristics of inversion MOS capacitors with different frequencies (10 kHz to 1 MHz) for n and p-type are reported. The correlation between inversion capacitance and field effect mobility at room and elevated temperatures are discussed as a new method to assess the quality of SiC/SiO_2 interface.

For the first time, the characteristics of 3D structures formed in silicon carbide for the realisation of ultra-high performance nanoscale transistors, based on the FinFET topology is investigated. C-V characteristics show evidence of a second flatband voltage, located at a higher bias than that seen for purely planar devices. Two distinct peaks in the conductance – voltage characteristics are observed, centered at the flatband voltages, where the peak located at high bias correlates with the behaviour of the sidewall area. This suggests that the chemical behaviour of the sidewalls differs from those of the (0001) wafer surface. The breakdown electric field of the dielectric film grown on the 3D structure is in excess of 3 $MVcm^{-1}$. It is demonstrated that 3D transistors (FinFETs) do not utilise the gate voltage range where the abnormal characteristics exist and so this work reports for the first time the possibility of high performance nanoscale transistors in silicon carbide that can operate at high temperatures.

LIST OF PUBLICATIONS

1. M. H. Weng, **M. I. Idris** et al, 2016. 'Analytical evaluation of thermally oxidized and deposited dielectric in NMOS-PMOS devices'. *Material Science Forum*, 858, p.631-634.

2. N. S .Mohamed, **M. I. Idris**, N. G. Wright and A.B. Horsfall, 2017. 'Silicon Carbide radiation detectors for medical applications'. In *Materials Science Forum*, (Vol. 897, pp. 626-629). Trans Tech Publications.

3. **M. I. Idris**, M. H. Weng, H.-K. Chan, A.E. Murphy, D. T. Clark, R. A. R. Young, E. P. Ramsey, N. G. Wright and A.B. Horsfall, 2016. 'Instability of phosphorus doped SiO_2 in 4H-SiC MOS capacitors at high temperatures'. *Journal of Applied Physics*, 120(21), p.214902.

4. **M. I. Idris** et al, 2017. 'Electrical stability impact of gate oxide in channel implanted SiC NMOS and PMOS transistors'. In *Materials Science Forum* (Vol. 897, pp. 513-516). Trans Tech Publications.

5. M. H. Weng, D.T. Clark, N. G. Wright, D. L. Gordon, M. A. Duncan, S. J. Kirkham, **M. I. Idris** et al, 2017. 'Recent advance in high manufacturing readiness level and high temperature CMOS mixed-signal integrated circuits on silicon carbide'. *Semiconductor Science and Technology*, 32(5), p. 054003.

6. **M. I. Idris** et al, 2017. 'Effect of post oxide annealing on the electrical and interface 4H-SiC/Al_2O_3 MOS capacitors'. In *Materials Science Forum* (accepted). Trans Tech Publications.

7. **M. I. Idris** et al, 2017. 'Enhanced oxide capacitance of 3-Dimentional 4H-SiC MOS capacitor'. In *Materials Science Forum* (accepted). Trans Tech Publications.

Contents

1 Introduction **1**

1.1 Introduction 1

1.2 Motivation 2

1.3 Thesis outline 3

1.4 Key contributions 5

2 A review of interface state density in 4H-SiC MOS devices **6**

2.1 Introduction 6

2.2 Overview of silicon carbide 7

2.2.1 History 7

2.2.2 Properties of SiC 8

2.2.3 Crystal of SiC (Polytype) 9

2.3 Future potential of the SiC technology 11

2.4 Key issues and challenges with SiC technology 12

2.4.1 Oxidation of 4H-SiC 12

2.4.2 Deposited SiO_2 15

2.4.3 Post oxide annealing 16

2.4.4 Recent advances in higk-κ dielectric technology for SiC MOSFET . . . 19

2.4.5 High-κ dielectric; aluminium oxide, Al_2O_3 22

2.4.6 Interface state density 26

2.5 The MOS capacitor 27

2.5.1 MOS Fundamentals 27

2.5.2 MOS capacitor 28

2.5.3 Non-ideal MOS capacitor 32

2.5.4 Compensation of C-V measurement (series resistance) 34

2.5.5 Extraction of interface state density 34

2.6 MOSFETs . . . 39
2.6.1 Field effect mobility in SiC MOSFETs and scattering mechanisms . . . 41
2.6.2 Correlation between subthreshold slope and interface state density . . . 43
2.6.3 Interface properties of the oxide / SiC interface on different crystallographics faces . . . 44
2.7 Multi-gate transistor/ FinFET . . . 45
2.7.1 Etching . . . 47
2.8 Summary . . . 47

3 Phosphorus doped SiO_2 / 4H-SiC MOS capacitors 49
3.1 Introduction: Instability of phosphorus doped SiO_2 in 4H-SiC MOS capacitors at high temperatures . . . 49
3.1.1 Experimental and evaluation method . . . 51
3.1.2 Results and discussion . . . 53
3.1.3 Flatband voltage, V_{FB} instability . . . 57
3.1.4 Threshold voltage, V_{TH} instability . . . 61
3.1.5 Total effective oxide charge density, N_{EFF} in phosphorus incorporated oxide . . . 63
3.1.6 Bias Temperature Stress (BTS) . . . 64
3.1.7 Interface Trap Density, D_{it} . . . 67
3.2 Positive flatband voltage shift in phosphorus doped N-type 4H-SiC MOS capacitors under constant voltage stressing, (CVS) . . . 70
3.2.1 Experimental . . . 73
3.2.2 Results . . . 74
3.3 Discussion . . . 81
3.3.1 Conclusion . . . 84

4 Influence of dielectric formation on the characteristics of 4H-SiC CMOS devices 86
4.1 Introduction . . . 86
4.2 Experimental: Processing techniques for the formation of dielectric . . . 86
4.3 SiO_2/SiC interface and impact of process variation . . . 88
4.3.1 Impact of the dielectric formation on the characteristics of n-type MOS capacitor . . . 88
4.3.2 Impact of the dielectric formation on the characteristics of p-type MOS capacitor . . . 93

4.4 Impact of elevated temperatures on MOS capacitors 97
4.4.1 Temperature dependence for n-type MOS capacitors 97
4.4.2 Temperature dependence for p-type MOS capacitors 101
4.5 Impact of dielectric formation and processing on SiC MOSFETs at RT 103
4.5.1 Comparison for n-channel MOSFETs at room temperature 105
4.5.2 Comparison for p-channel MOSFETs 105
4.6 Impact of dielectric formation and processing on SiC MOSFETs at elevated temperatures 107
4.6.1 Temperature dependence for n-channel MOSFETs 107
4.6.2 Temperature dependence for p-channel MOSFETs 109
4.7 Inversion MOS capacitor 112
4.7.1 Correlation of inversion capacitance with field effect mobility at RT . . 116
4.7.2 Correlation of inversion capacitance with field effect mobility (n-channel) at high temperature 117
4.7.3 Correlation of inversion capacitance with field effect mobility (p-channel) at high temperature 120
4.7.4 Correlation of inversion capacitance with field effect mobility (Discussion) 122
4.8 Summary 123

5 3D Structures for Silicon Carbide Transistors 126

5.1 Fabrication and characterization of 3-Dimensional MOS capacitors 4H-SiC by PECVD as gate dielectric 126
5.1.1 Device fabrication 128
5.1.2 Result and Discussion 129
5.1.3 3-D MOS capacitors with different off angles 134
5.2 3-Dimensional 4H-SiC MOS capacitors grown by atomic layer deposition of Al_2O_3 137
5.2.1 Experiment and evaluation method 139
5.2.2 Results and Discussion 139
5.2.3 Summary 145
5.3 Analysis of 3-Dimensional 4H-SiC MOS capacitors grown by atomic layer deposition of Al_2O_3 at high temperatures 146
5.4 Effect of post oxidation annealing (POA) on the 3D MOS capacitor 147

5.4.1 Effect of post-oxide annealing on the electrical and interface 4H-SiC/SiO_2 3D MOS capacitors 147
5.4.2 Effect of post-oxide annealing on the electrical and interface of 4H-SiC/Al_2O_3 3D MOS capacitors 149
5.4.3 Experimental 151
5.4.4 Result and Discussion 152
5.5 Conclusion 156

6 Conclusions and future work **158**
6.1 Summary 158
6.2 Future work 159

List of Figures

2.1 The diameter size of silicon carbide wafers demonstrated in Research and Development at Cree Research (Wolfspeed). 8

2.2 The stacking sequences of double layers of a) 3C, (b) 4H and (c) 6H SiC from the side view of $(11\bar{2}0)$ direction. 11

2.3 Applications area of SiC devices including low, medium and high voltage . . . 12

2.4 DLTS spectra showing the generation of ON1 and ON2 defects after oxidation on n-type 4H-SiC at 1300°C for 1.3h. 14

2.5 TMA molecules reating with the -OH groups on the substrate. 25

2.6 H_2O molecules react with the TMA molecule fragments attached to the substrate surface. 25

2.7 Cross section TEM image of Al_2O_3 deposited by ALD on trench structure of silicon 26

2.8 (a) Illustration of the distribution of interface state density within the bandgap of 4H-SiC and 6H-SiC. (b) Interface states system at oxide/semiconductor interface including donor-like and acceptor-like state with in bandgap. 27

2.9 Schematic cross-section of an (a) Ideal Metal-Insulator-Semiconductor (MIS) capacitor and (b) the equilvalent circuit. 28

2.10 Schematic of ideal MOS capacitor energy band diagram under equillibrium conditions. 29

2.11 Normalized C-V curve for p-type MOS capacitor with different type of frequencies. 29

2.12 Energy band diagrams for p-type MOS structure in different region (a) accumulation, (b) depletion and (c) inversion. 32

2.13 Type of charges associated with non-ideal MOS capacitor. 33

2.14 Equivalent circuit for conductance measurement; (a) Including interface trap effects, $C_{\rm it}$ and $R_{\rm it}$, (b) simplified circuit of (a), (c) measured circuit. 36

2.15 Equivalent circuit for low frequency and high frequency. 37

2.16 Equivalent circuit for a MOS capacitor using C-ψ_{s} method (a) in depletion (b) strong accumulation where C_{D}, C_{OX}, C_{it}, G_{PIT} and Z are the semiconductor capacitance, oxide capacitance, interface-state capacitance, interface-state conductance and parasitic impedance respectively. 39

2.17 Schematic of n-channel MOSFET device structure on p-type substrate 40

2.18 Scattering mechanisms that are affecting the field effect mobility in MOSFET. . 43

2.19 Transfer characteristic (I_{D}-V_{G}) with and without D_{it}. 44

2.20 Field effect mobility as a function of oxide field on n-channel MOSFETs fabricated on 4H-SiC with different face orientation of (0001), (000$\bar{1}$) and (11$\bar{2}$0) 45

2.21 SEM image of FinFET with multi fins at a 120 nm pitch using e-beam lithography 46

2.22 Reactive ion etching (RIE) using photoresist as a mask. 47

3.1 Room temperature C-V characteristics of 4H-SiC MOS capacitors (a) undoped gate dielectric (b) phosphorus doped gate dielectric. Experimental quasi–static and high frequency (1MHz) data are plotted with a theoretical curve. 55

3.2 1MHz Capacitance Voltage characteristics of undoped (a) and phosphorus doped devices (b) measured at temperatures between 100°C and 300°C. 56

3.3 1MHz bidirectional Capacitance Voltage characteristics (hysteresis) of (a) undoped devices at room temperature (b) undoped devices at 300°C (c) phosphorus doped devices at room temperature (d) phosphorus doped devices at 300°C. 57

3.4 Change in flatband voltage ΔV_{FB} extracted from 1 MHz C-V characteristics as a function of temperature for undoped and phosphorus doped dielectrics under (a) negative and (b) positive gate bias conditions. ΔV_{FB} is defined as the difference of V_{FB} at room temperature and those V_{FB} obtained at elevated temperature. 58

3.5 Frequency dependence of V_{FB} for the phosphorus doped oxide measured for both directions. Forward sweep Figure (a) and reverse sweep Figure (b). . . . 60

3.6 Threshold voltage (ΔV_{TH}) extracted from 1 MHz C-V characteristics as a function of temperature for the undoped (sample 1) and phosphorus doped (sample 2) dielectrics under (a) negative and (b) positive gate bias conditions. . 62

3.7 Frequency dependence of V_{TH} for sample 2 measured for both directions. Forward sweep figure (a) and reverse sweep figure (b). 63

3.8 Variation in effective oxide charge density in sample 1 and 2 under negative (a) and positive (b) gate bias conditions. 65

3.9 C-V curves illustrating the effect of mobile charge motion for undoped (a) and phosphorus doped dielectric (b) measured before (solid lines) and after (dash lines) PBTS. 66

3.10 C-V curves illustrating the effect of mobile charge motion for undoped (a) and phosphorus doped dielectric (b) measured before (solid lines) and after (dash lines) NBTS. 68

3.11 Comparison of interface state density ($D_{\rm it}$) as a function of energy, extracted using the C-ψ_s technique. 69

3.12 Interface state density ($D_{\rm it}$) as a function of energy at varying temperatures extracted using Terman method for sample1 (a) and sample 2 (b). 71

3.13 Electrons injection into the oxide by means of FN tunneling under high electric field. (Accumulation region for n-type MOS capacitor) 75

3.14 J-E characteristics of sample 1 and sample 2 at room temperature and 100°C under positive bias (accumulation region for n-type MOS capacitor). 76

3.15 FN plots of (a) undoped and (b) phosphorus-doped SiO_2 samples at room temperature and 100°C. 77

3.16 Shift in flatband voltage, $\Delta V_{\rm FB}$ and effective oxide charge density, $\Delta N_{\rm EFF}$ under different gate bias stress times at the room temperature (a and b respectively) and 250°C (c and d respectively) extracted from 1 MHz C-V curves. $\Delta V_{\rm FB}$ is defined as the difference of $\Delta V_{\rm FB}$ without bias stress time and those $\Delta V_{\rm FB}$ obtained at different bias stress time. 78

3.17 Shift in flatband voltage (a) and effective oxide charge density (b) at room temperature under different gate bias conditions. Shift in flatband voltage (c) and effective oxide charge density (d) at high voltage ($\pm$ 30 V) held with different bias stress time up to 999 s. 80

3.18 The changes of $\Delta D_{\rm it}$ as a function bias stress time for sample 1 and sample 2 under reverse sweep measured from V_g= 30V at room temperature. 81

3.19 Mobile charges are moved to near interface as the constant high voltages are applied with certain bias stress time. 82

4.1 Schematic cross section of the SiC a) n-MOS capacitors and b) p-channel MOSFET on n-epilayer. 87

4.2 (a) 1 MHz Capacitance-Voltage characteristics (b) Normalised 1 MHz Capacitance-Voltage characteristics for n-type MOS capacitor with different dielectric formation (Sample A, B and C). 89

4.3 Interface state density as a function of energy extracted by C-ψ technique for n-type MOS capacitors. 90

4.4 Current density- Electric Field, J-E for n-type MOS capacitors with different dielectric formation in accumulation. The area of MOS capacitors are 1.35×10^{-3} cm^2. 91

4.5 FN-plots for n-type MOS capacitors obtained from current-voltage measurements. From the slope, barrier heights of 2.4 to 2.5 eV were extracted. These values are close to the theoretical value of 2.7 eV. 92

4.6 (a) 1 MHz Capacitance-Voltage characteristics (b) Normalised 1 MHz Capacitance-Voltage characteristics for p-type MOS capacitor with different dielectric formation (Sample A, B and C) 93

4.7 Interface state density as a function of energy extracted by C-ψ method for p-type MOS capacitors. 94

4.8 Current density- Electric Field, J-E for p-type MOS capacitors with different dielectric formation in accumulation. The area of MOS capacitors are 1.35×10^{-3} cm^2. 95

4.9 FN-plots for p-type MOS capacitors at room temperature. From the slope, a barrier heights of 1.48 to 2.18 eV are extracted. These values are quite far from the theoretical value of 2.9 eV. 96

4.10 1 MHz Capacitance-Voltage characteristics for Sample A (a), B (b) and C (c) n-type MOS capacitor from RT to 400°C. 98

4.11 Variation of (a) $V_{\rm FB}$ and (b) $N_{\rm EFF}$ for all sample n-type MOS capacitor from RT to 400°C. 99

4.12 Interface state density as a function of energy for Sample A (a), B (b) and C (c) n-type MOS capacitor from RT to 400°C. 100

4.13 Illustration of bandgap narrowing effect from room temperature to high temperature. The position of Fermi level moves toward midgap with increase in temperature results in a reduction of interface state density. 101

4.14 1 MHz Capacitance-Voltage characteristics for Sample A (a), B (b) and C (c) p-type MOS capacitor from RT to 400°C. 102

4.15 Variation of (a) V_{FB} and (b) N_{EFF} for all sample p-type MOS capacitor from RT to 400°C. 103

4.16 Interface state density as a function of energy for Sample A (a), B (b) and C (c) p-type MOS capacitor from RT to 400°C. 104

4.17 Comparison of field effect mobility as a function of voltage for n-channel samples A, B and C at room temperature. The size of transistor is L_G=1.2 μm, W_G=200 μm. The field effect mobility was extracted from data of I_{D}-V_{G} measured at room temperature with V_{D}=0.1 V. 106

4.18 Comparison of field effect mobility as a function of voltage for p-channel samples A, B and C at room temperature. The size of transistor is L_G=1.2 μm, W_G=200 μm. The field effect mobility was extracted from data of I_{D}-V_{G} measured at room temperature with V_{D}=-0.1 V. 106

4.19 Change in peak field effect mobility of n-channel MOSFET for sample A, B and C from RT to 400°C. 108

4.20 Change in threshold voltage, V_{TH} of n-channel MOSFET for sample A, B and C from RT to 400°C. 108

4.21 Substhrehold swing characteristics of n-channel MOSFET for sample A, B and C from RT to 400°C. 109

4.22 Change in peak field effect mobility of p-channel MOSFET for sample A, B and C from RT to 400°C. 110

4.23 Change in threshold voltage, V_{TH} of p-channel MOSFET for sample A, B and C from RT to 400°C. 111

4.24 Subthrehold swing characteristics of p-channel MOSFET for sample A, B and C from RT to 400°C. 112

4.25 Schematic of p-type inversion MOS capacitor SiC from the (a) top view (b) cross section. 113

4.26 C-V characteristics of n-type 4H-SiC inversion MOS capacitor with different frequency from 10 kHz to 1 MHz for sample A at room temperature. The measurements were swept from accumulation to inversion (a) and vice versa (b) at 0.1 V/s in a dark box. 114

4.27 C-V characteristics of p-type 4H-SiC inversion MOS capacitor with different frequency from 10kHz to 1MHz for sample A at room temperature. The measurements were swept from accumulation to inversion (a) and vice versa (b) at 0.1 V/s in a dark box. 114

4.28 The change in inversion capacitance, C_{INV} wth different frequencies at gate votage, V_{G}= 15V for both n and p-type inversion MOS capacitor for sample A at room temperature due to the minority carrier response. The measurements were swept from accumulation to inversion (a) and vice versa (b) at 0.1 V/s in a dark box. 116

4.29 (a) Normalized 1 MHz C-V characteristics of p-type 4H-SiC inversion MOS capacitor for samples A, B and C at room temperature. The measurements were swept from accumulation to inversion at 0.1 V/s in a dark box. (b) Comparison of field effect mobility as a function of gate overdrive for n-channel samples A, B and C at room temperature. The size of transistor is L_G=1.2 μm, W_G=200 μm. The field effect mobility was extracted from data of I_{D}-V_{G} measured at room temperature with V_{D}=0.1 V. 118

4.30 Normalized 1 MHz C-V characteristics of n-type 4H-SiC inversion MOS capacitor for sample A, B and C at room temperature. The measurements were swept from accumulation to inversion at 0.1 V/s in a dark box. (b) Comparison of field effect mobility as a function of gate overdrive for p-channel samples A, B and C at room temperature. The size of transistor is L_G=1.2 μm, W_G=200 μm. The field effect mobility was extracted from data of I_{D}-V_{G} measured at room temperature with V_{D}=-0.1 V. 118

4.31 The temperature dependence of inversion capacitance (p-type inversion MOS capacitor) at strong inversion and field effect mobility for sample (a) A, (b) B and (c) C (n-channel MOSFET). 119

4.32 The temperature dependence of inversion capacitance (n-type inversion MOS capacitor) at strong inversion and field effect mobility for sample (a) A, (b) B and (c) C (p-channel MOSFET). 121

4.33 The correlation between field effect mobility with inversion capacitance for (a) p-type inversion MOS capacitor/ n-channel MOSFET and (b) n-type inversion MOS capacitor/ p-channel MOSFET. 122

4.34 (a) Field effect mobility (b) inversion capacitance as a function of voltage at peak mobility. 123

5.1 Schematic diagram of the cross-section of 3D MOS capacitors (top) and the illustration of mask design for 3-D MOS capacitors (below). 129

5.2 Process flow of the fabrication of 3-D MOS capacitors. 130

5.3 SEM images of a) Surface roughness of trench on sidewall, b) 3-D MOS capacitor before metallization, c) Cross-section, d) 3-D trench after metallization. 131
5.4 C-V curves of 3-D MOS MOS capacitors with different trench sizes measured at 1 MHz. For example, T10B10 is a 3D MOS capacitor device with a width of 10 μm on the top and bottom trench. 132
5.5 G-V curves of 3-D MOS MOS capacitors with different trench sizes measured at 1 MHz. 133
5.6 Changes of oxide capacitance, C_{OX} (accumulation region) with different the trench sizes. 133
5.7 Increment of oxide capacitance, ΔC_{OX} with additional area on the sidewalls. . 134
5.8 Interface state density as a function of energy of 3-D MOS capacitors with different trench sizes. 135
5.9 Oxide capacitance of 3-D MOS capacitors on different off angles. 135
5.10 Interface state density as a function of energy for 3-D MOS capacitors on different off angles extracted using Terman method. 136
5.11 Schematic illustration of the cross-section of 3-D gate structure MOS capacitor. 139
5.12 SEM images of a typical 3-Dimentional gate structure of 3-D MOS capacitor formed by RIE using Ti/Ni as a mask. 140
5.13 1 MHz C-V and G-V characteristics of 3D MOS capacitors at room temperature. 141
5.14 Variation in capacitance and conductance with sidewall surface area. 142
5.15 The distribution of interface state density as a function of energy within the bandgap, extracted using the $C - \psi$ technique for 3D MOS capacitors with different sizes. Planar capacitors of etched and non-etched were also included in the figure as a reference. 143
5.16 Interface state density of 3-D MOS capacitors near conduction band, $E_c - E$=0.2 eV as a function of sidewall area, extracted using $C - \psi$ technique. . . . 144
5.17 Leakage current density through the Al_2O_3 film, for both planar and 3D structures. 146
5.18 Change in oxide capacitance from 1 MHz C-V characteristics as a function of temperature for 3-D MOS capacitors showing samples with different trench sizes. 148
5.19 Change in flatband voltage from 1 MHz C-V characteristics as a function of temperature for 3-D MOS capacitors. 148
5.20 C-V characteristic of 3-D MOS capacitors with different annealing. 150
5.21 G-V characteristic of 3-D MOS capacitors with different annealing. 150

5.22 Interface state density of 3-D MOS capacitors with different annealing. 151
5.23 Hysteresis of samples with different annealing temperatures. Change in oxide capacitance of samples with different annealing temperatures. 153
5.24 Change in flatband voltage, V_{FB} for samples as a function of the number of measurements. The measurements were repeated on the same samples. 153
5.25 V_{FB} shift as a function of the starting voltage. Gate voltage of 5, 7 and 10 V were applied from the accumulation region to depletion region. 154
5.26 Interface trap density, $D_{\rm it}$ as a function of energy at room temperatue. C-ψ technique was used to extract the interface trap density, $D_{\rm it}$. 155
5.27 Current density- Electric field (J-E) characteristic of Al_2O_3/SiC MOS capacitors annealed at different temperatures. 155

List of Tables

2.1 Comparison of the materials properties of Si, 3C-SiC, 4H-SiC, 6H-SiC, GaN and diamond at 300 K 10

2.2 Summary of important parameters for n-channel SiC MOSFET with different gate dielectric formation. 20

2.3 Summary of potential high-k material. 22

2.4 Summary of important parameters of SiC MOSFET utilizing Al_2O_3 as a gate dielectric. 24

3.1 Summary of fabrication process for both samples. 52

4.1 Description of the processing steps used in the fabricarion of the dielectrics in sample A, B and C. 88

4.2 Summary of parameters extracted from n-type MOS capacitors. 88

4.3 Summary of parameters extracted from p-type MOS capacitors. 93

5.1 Summary of the size parameters for 3-D MOS capacitors. 130

Abbreviations

AC	alternating current
ALD	atomic layer deposition
Al_2O_3	aluminum oxide
AlN	aluminum nitride
B	boron
BN	boron nitride
BSG	borosilicate glass
BTS	bias temperature stress
CH_4	methane
CO_2	carbon dioxide
CVD	chemical vapor deposition
CVS	constant voltage stress
CMOS	complementary metal oxide semiconductor
CVD	chemical vapor deposition
C-V	capacitance versus voltage
DC	direct current
DFT	density function theory
DIBL	drain induced barrier lowering
ECR	electron cyclotron resonance
EOT	equivalent oxide thickness
FinFET	fin field effect transistor
FN tunnelling	Fowler-Nordheim tunnelling
GaN	gallium nitride
GaAs	gallium arsenide
HfO_2	hafnium dioxide
High-κ	high-kappa
HTA	high temperature annealing
ICP	inductively coupled plasma
InP	indium phosphide
ITRS	international technology roadmap for semiconductors
I-V	current versus voltage
J-E	current density versus electric field
KTP	knowledge transfer program

$LaSiO_x$	lanthanum silicate
La_2O_3	lanthanum oxide
LSI	large scale integration
MIS	metal insulator semicondutor
MOS	metal-oxide-semicondutor
MOCVD	metal organic chemical vapor deposition
MOSFET	metal oxide semiconductor field effect transistor
N_2	nitrogen
NBTS	negative bias temperature stress
NO	nitric oxide
N_2O	nitrous oxide
PBTS	positive bias temperature stress
PDA	post-deposition annealing
PECVD	plasma enhanced chemical vapor deposition
PMA	post metallisation annealing
POA	post-oxide annealing
$POCl_3$	phosphoryl chloride
PSG	phosphosilicate glass
PVD	physical vapour deposition
PVT	physical vapour transport
P_2O_5	phosphorus pentoxide
RCA	Radio Corporation of America
RIE	reactive ion etching
RMS	root mean square roughness
RF	radio frequency
RTP	rapid thermal annealing
SCE	short-channel effect
SEM	scanning electron microscopy
SiC	silicon carbide
SiN_x	silicon nitride
SiO_2	silicon dioxide
SSRM	scanning spreading resistance microscopy
TEM	transmission electron microscopy
TMA	trimethylaluminum

TVS	triangular voltage sweep
XPS	x-ray photoelectron spectroscopy

Nomenclature

A	area
C_{FB}	flatband capacitance
C_{OX}	oxide capacitance
C_{M}	measured capacitance maxima
C_{m}	measured capacitance
C_{t}	total capacitance
C_{dep}	semiconductor depletion layer capacitance
C_{inv}	inversion capacitance
C_{s}	semiconductor capacitance
D_{it}	interface trap density
E_{C}	conduction band energy
E_{F}	Fermi energy
E_{G}	bandgap energy
E_{i}	intrinsic energy
E_{V}	valence band energy
Q_{it}	interface trap charge
E	electric field
$\varepsilon_{\mathrm{ox}}$	dielectric permittivity
μ_{FE}	field effect mobility
ε_0	permitivity of free space
ε_{s}	semiconductor permittivity
G_{ma}	measured conductance maxima
k_{B}	Boltzman constant
L_{D}	Debye length
m_{e}/m^*	effective carrier masses
n_{i}	intrinsic carrier concentration
N_{A}	acceptor impurity concentration
N_{D}	donor impurity concentration
N_{it}	near interface trap
N_{EFF}	effective oxide charge concentration
N_{ot}	slow oxide trap
ω	angular frequency
ϕ_{B}	potential barrier height

Φ_{B}	bulk potential
Q_{EFF}	effective oxide charge
Q_{f}	fixed oxide charge
Q_{m}	mobile charge
Q_{ot}	oxide trap
R_{s}	series resistance
S	subthreshold swing
σ_{n}	capture cross-section
t_{OX}	oxide thickness
V_{FB}	flatband voltage
V_{TH}	threshold voltage
V_{bi}	built-in potential
W_{MS}	metal-semiconductor work function

Chapter 1

Introduction

1.1 Introduction

In the world of electronic devices, silicon technology has been dominating the industry since the invention of the transistor. Silicon is one of the most abundant elements in nature and high quality substrates are easily available. However, the devices have reached the physical limits in a vast number of application areas such as at high voltage, high temperature and high radiation environment where silicon devices are incapable of performing. Compound semiconductors are becomming the material of choice in these applications where silicon devices exhibit poor performance owing to intrinsic material properties. For example, gallium arsenide (GaAs) and indium phosphide (InP) have been extensively used for high frequency devices and light emitting devices. As our society continues to advance scientifically, numerous demands for semiconductor devices that can be operated at high temperature have arisen. For such applications, wide band gap semiconductors are a viable solution to conventional silicon-based electronics. Silicon carbide (SiC) is a promising candidate for extreme environment electronics due to its unique physical and chemical properties. It has a strong bonding between Si and C that results in a hard and strong material.

Due to its superior properties coupled with the availability of high quality commercial wafers, SiC is an ideal semiconductor to replace Si for high temperature applications. SiC is the only wide band gap that can form SiO_2 as a native oxide, which is an important advantage in device fabrication. However, the physical and chemical stability of SiC makes the crystal growth of SiC extremely complex and restricts the development of SiC semiconductor devices and electronic applications. The presence of diverse SiC structures with different stacking sequences (different polytype), such as 3C-, 4H- and 6H-SiC has also delayed the growth of electronic grade SiC crystals.

Part of the investigation undertaken within this thesis is a collaboration between the research group at Newcastle University and Raytheon UK which was funded as part of a knowledge transfer program (KTP). The work reported in this thesis focuses on the characterization and understanding of 4H-SiC MOS devices, with the intention to reduce the interface state

density and improve the stability device performances. All of the experimental results and data extracted from the devices discussed in this thesis were conducted at Newcastle University by the author unless stated otherwise.

1.2 Motivation

The demand for electronic devices that are capable of operating in harsh environments is increasing rapidly. Silicon is the most commonly used semiconductor for electronic devices. The progress in large scale integration (LSI) and advanced simulation technology had a significant impact on the development of electronic devices. However, current silicon device technology is relatively established and it is difficult to achieve a significant breakthrough. Silicon carbide (SiC) is an excellent wide band gap semiconductor for high power, high temperature, or high-speed switches owing to its superior material properties such as a high breakdown voltage, which is ten times higher than that of silicon, high electron mobility, and thermal conductivity [1]. The advantage of SiC is that it is the only wide band gap compound semiconductor that can produce high quality of SiO_2 layer by thermal oxidation which makes it an ideal candidate for applications where conventional silicon technology cannot function, which is the main focus of this research. This developing SiC technology offers a significant impact in many industrial sectors including aerospace, automotive, oil and gas and communications. This emerging technology is also a promising material for advanced power devices. For example, the automotive industry is developing environmentally friendly vehicles also known as hybrid vehicles to reduce the carbon dioxide (CO_2) pollution and conserve fossil fuels. Due to the high saturation drift velocity and high temperature operation, SiC has become a component in high volumetric density performance power electronic circuits.

An inversion layer mobility, of about 3 times higher than that achieved with NO annealing on the Si-face was achieved by post oxide annealing in phosphoryl cloride ($POCl_3$) [2]. It was found that phosphorus incorporation turns SiO_2 to phosphosilicate glass (PSG) and reduced the interface state density at the interface, hence improve the channel mobility of SiC MOSFETs. However, PSG is a polar material and can lead to threshold voltage instability [3, 4]. The PSG film presence considerably changes the character of charge state in MOS structures under both polarities. Negative bias induces positive PSG polarization charge at the interface (negative shift in V_{FB}). The positive shift in V_{FB} is due to induced negative polarize charge. To date, there is no report on the stability of phosphorus doped SiO_2 MOS capacitors at high temperatures. Although phosphorus incorporation has successfully improved the channel

mobility of 4H-SiC MOSFETs, the stability of device performance at high temperatures is of critical importance because one of the key advantages of SiC devices is the capability to operate in extreme environments.

In an effort to increase the channel mobility, a 3-Dimensional MOS capacitors has been fabricated and characterised. Through an innovative FinFET structure, 3D-MOS capacitors enhance the oxide capacitance, due to larger total surface area from the sidewall areas, and show a reduction in the interface state density as different plane orientation on the sidewall. In silicon technology, the 3-D gate structure or FinFET has emerged as a novel device having superior control over short channel effects. It is a promising alternative to planar devices in the sub 50 nm generation due to increased gate control from three sides of the active areas.

The commercial availability of single crystalline 4H-SiC wafers over the past 20 years has created a great deal of interest in SiC device applications. Wafer quality has gradually increased along with wafer diameter and offers a significant opportunity for the development and manufacture of commercial devices and circuits. Today, SiC wafers up to 200 mm diameter with an excellent surface profile in term of surface roughness are available in the market at reasonable price [5].

1.3 Thesis outline

Although great efforts have been made to develop SiC MOSFETs, there are still some problems for their practical use. The presence of a large interface state density, D_{it} and surface roughness in the thermally grown SiO_2/SiC interface are the main problems. The focus of this thesis is on improving the channel mobility and the stability of flatband voltage which are the main problem in SiC MOSFETs.

Chapter 2: Literature review: A review of 4H-SiC MOS and MOSFETs

Chapter 2 comprises a literature review of the history and material properties of 4H-SiC. The key issue and challenges in SiC technology are described starting from the oxidation of 4H-SiC, post oxide annealing and recent development in high-κ materials. The fundamental theory of MOS capacitor and MOSFET followed by the extraction techniques of interface state density and the future potential of SiC technology are discussed in this chapter.

Chapter 3: The instability of phosphorus doped SiO_2 4H-SiC MOS capacitors at high temperatures and high electric field.

A comparison between phosphorus doped and as-grown oxide layers has been made to see the effect of phosphorus incorporation at high temperatures. C-V and I-V measurements were performed to extract parameters including flatband voltage, threshold voltage, effective oxide charge and interface state density. The origin of the positive flatband voltage in phosphorus doped N-type 4H-SiC MOS capacitors at high temperature and high electric field was investigated under different bias times and conditions.

Chapter 4: Influence of dielectric formation on the characteristics of 4H-SiC CMOS devices

In this chapter, the electrical characteristics of 4H-SiC CMOS capacitor and transistor structures have been compared to the recently developed inversion MOS capacitor structure to investigate the influence of dielectric formation on the characteristics of 4H-SiC CMOS devices. The temperature dependence of important parameters including the flatband voltage, effective oxide charge and interface state density for MOS capacitors and the field effect mobility, threshold voltage and substhreshold swing for MOSFETs was examined in this section to study the effect of different dielectric formation at elevated temperatures. An investigation on the characteristics of inversion MOS capacitors for n and p-type were also conducted. The correlation between inversion capacitance and field effect mobility at room and elevated temperatures is discussed as a new method to assess the quality of the SiC/SiO_2 interface.

Chapter 5: 3D Structures for Nanoscale Silicon Carbide Transistors

The move to short gate length transistors is not possible in high temperature electronics using conventional transistor structures. The excess carriers that are generated at high temperatures results in the ability of the gate to modulate the current flow being severely impaired. This is often described as a loss of electrostatic integrity, an issue faced by nanometer scale silicon transistors in modern integrated circuits. By moving to 3D structures, often labelled as FinFETs, it is possible to increase the electrostatic integrity of the device and this will enable the channel length of the device to shrink, whilst maintaining the electrical characteristics. The intention of this work is to demonstrate, for the first time, that the use of 3D structures in silicon carbide is a key enabling technology in the realisation of short gate length transistors for high performance logic circuits that can operate in high temperature environments.

Chapter 6: Conclusion and future work

Chapter 6 summarises the key findings, technical investigations and suggestions for future works.

1.4 Key contributions

The investigations that have been carried out within this thesis provide several key contributions to the research community including:

- Experimental measurements and data analysis of phosphorus doped SiO_2 4H-SiC MOS capacitors at high temperatures up to 300°C
- Electron tunneling mechanism in the high electric field of phosphorus doped SiO_2 4H-SiC MOS capacitors
- A comparison study of n-type and p-type MOS capacitors and MOSFET with different dielectric formation
- Analysis of inversion MOS capacitor on both n and p-type 4H-SiC including the correlation between inversion capacitance and field effect mobility at room and high temperature.
- Fabrication and characterisation of 3-Dimensional MOS capacitors using different dielectric formation

Chapter 2

A review of interface state density in 4H-SiC MOS devices

2.1 Introduction

In recent decades, there has been an increasing demand for new semiconductor materials that can operate in extreme environments where standard silicon electronics fail to function. These conditions include high temperatures, high power density, high voltage applications and high radiation conditions [6, 7]. Furthermore, owing to demands for sustainable energy production and reduction in carbon emissions worldwide, the use of high-performance electronics has become critical to a wide range of industrial sectors including automotive, aerospace, military and nuclear power generation. Existing devices made of silicon are approaching the theoretical limit for operation as determined by its material properties; at high temperature, the material becomes intrinsic and fails as it is no longer able to block the voltage. Therefore, wide bandgap semiconductors such as silicon carbide (SiC), gallium nitride (GaN) and aluminum nitride (AlN) are viable alternative solutions for such applications, due to their superlative materials properties.

SiC is an interesting material for electronic devices. In comparison to silicon, SiC features excellent physical and chemical properties (refer Table 2.1) that allow it to operate in extreme environments. Interestingly, in general terms, the fabrication process of SiC devices is similar to silicon technology. Therefore, SiC can be adopted to silicon technology production line simply and without excessive cost. The ability to be oxidized at elevated temperatures gives SiC a significant advantage compared to other wide bandgap semiconductors. The thermal oxide grown on SiC is similar to silicon in terms of dielectric strength and bandgap. However, the quality of the SiC/SiO_2 interface is not as good as that formed betweenn Si and SiO_2, where the interface state density for as grown N-type 4H-SiC MOS capacitors is typically around 10^{13} $cm^{-2}eV^{-1}$ close to the conduction band [8, 9]. The presence of a large density of interface traps degrades the quality of MOSFET devices by capturing charged carriers and introducing Coulomb scattering that dominates the MOSFET characteristics at low electric field. The high density of interface states is also correlated to the instability of the threshold voltage, which is one of the main focuses in this study.

2.2 Overview of silicon carbide

Silicon carbide (SiC) is an excellent wide bandgap semiconductor for high power, high temperature, or high-speed switches owing to its superior material properties, such as high breakdown electric field (which is ten times superior to that of silicon), high electron mobility, and thermal conductivity [10–12]. The advantage of SiC is that it is the only wide bandgap semiconductor that can produce high-quality SiO_2 layers by thermal oxidation, which makes it an ideal candidate for metal-oxide-semiconductor applications; for example, logic circuits for microcontroller. Although significant efforts have been made to develop SiC MOSFETs, there are still some problems in terms of their practical use. The presence of a large interface state density, D_{it} and surface roughness in the thermally grown SiO_2/SiC interface are significant issues.

2.2.1 History

In 1824, Berzelius first reported the indentification of a compound containing silicon-carbon bonds, formed by passing a current through a carbon rod in the mixture of silica, carbon and some additives such as salt [13]. The first application of SiC was the production of SiC powders used for polishing, grinding and cutting [11]. In the meantime, natural SiC was discovered by Moissan as a mineral [11]; thus it is named ”Moissanite”. In 1955, Lely has successfully grown relatively pure SiC, mostly 6H-SiC crystals, by a sublimation technique [14]. This has facilitated SiC as a semiconductor for applications for high-temperature electronics. A modified Lely method, also known as physical vapour transport (PVT) was developed by M. Tairov and V.F. Tsvetkov [15]. They invented a reproducible method for SiC production based on thermodynamic and kinetic considerations by introducing a seed into a sublimation growth furnace. Several groups further developed a growth process to obtain a larger diameter and fewer defect of SiC wafer.

Production of an industrial volume of silicon carbide ingots is one of the challenging tasks faced by the SiC industry. Due to its physical and chemical nature, it is difficult to grow single crystals of SiC. Calculations indicate that extremely high-temperatures and high-pressure conditions are required to produce single crystalline materials [16]. Even a slight difference in enthalpy leads to the formation of different SiC polytypes. The seeded sublimation growth method, which uses a high quality crystal as a seed, is the most common method that has been used for SiC wafer production. This approach has become the standard industrial process and is able to

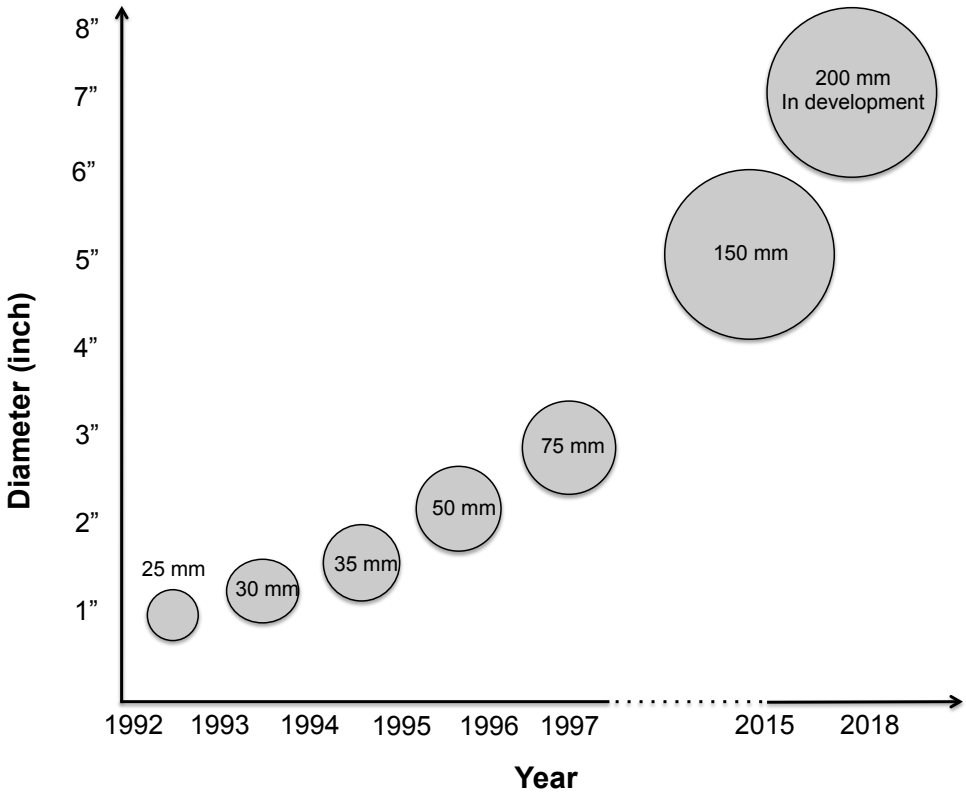


Figure 2.1: The diameter size of silicon carbide wafers demonstrated in Research and Development at Cree Research (Wolfspeed).

produce high quality and low defect (micro-pipes) SiC wafers with increasing diameter [17–19]. Fig 2.1 shows the progress of wafer size (in diameter) between 1992 and 2015. 150 mm diameter bulk SiC wafers are currently available and bigger wafers are anticipated to be available soon. The wafer size is crucial as it may reduce the cost of devices that can be produced when the wafer size increases further. Nevertheless, there are other methods such as high-temperature chemical vapour deposition (HT-CVD), continuous feed physical vapour transport (CF-PVT), Halide CVD (H-CVD) and modified PVT (M-PVT) still primarily at the research stage and will certainly draw more attention in the future [16, 20, 21].

2.2.2 Properties of SiC

SiC is a compound semiconductor, comprising a stoichiometry of 50% silicon (Si) and 50% carbon (C). Si and C atoms are tetrahedrally bonded with covalent bonds by sharing electron pairs in outer orbitals to form a SiC crystal. Each Si atom has exactly four C atom neighbor, and vice versa. The Si-C bond energy is very high, 360 kJ/mol (4.6 eV), which gives SiC the outstanding material properties. SiC has many polytypes (more than 200 are known) due

to the variation of the stacking sequence [14]. The primary crystallographic categories of SiC are cubic, hexagonal and rhombohedral. The polytypes are represented by the number of Si-C bilayers in the unit cell in Ramsdell's notation. The stacking sequences for most popular polytypes of SiC such as 2H-, 4H-, 6H-, 15R and 3C-SiC. Each polytype of SiC exhibits different electrical, mechanical, thermal and optical properties. The comparison of some important properties of SiC are due to different properties is shown in Table 2.1. For example, the bandgap of 4H-SiC is larger than that of 3-C and 6H-SiC. For that reason, 3C- SiC has been researched for non-electronic applications such as abrasive and cutting tools instead of power electronics application. 4H-SiC and 6H-SiC both have excellent physical properties, such as high breakdown voltage, high saturation velocity, and high thermal conductivity [22]. Nevertheless, 4H-SiC has substantially higher carrier mobility, relatively small mobility anisotropy and shallower dopant ionization energy in comparison to 6H-SiC, that make it the best polytype for electronic devices.

2.2.3 Crystal of SiC (Polytype)

As can be seen in Fig. 2.2 from the side view of $(11\bar{2}0)$ direction, 3C-SiC has a stacking sequence of ABCABC with a cubic crystal structure where a sequence of 3 different letters (ABC) indicates cubic type stacking. Meanwhile, 4H-SiC has 4 stacking sequences of ABCBABCB with the hexagonal crystal structure where for example a letter C is in between 2 letter B indicates hexagonal type stacking. Ramsdell notation is commonly used to define the polytype of SiC. For example, 4H-SiC refers to 4 bilayers of Si and C and it is hexagonal crystal structure. 3C refers to 3 bilayers in its cubic crystal structure. Miller or Miller-Bravais indices are used to describe the directions in all SiC polytypes. The first three indices in Miller-Bravais represents the directions in the basal plane (perpendicular to c-axis). The angle between two adjacent basal plane axis is 120°. The representation of a plane (h, k, i, l) requires that the sum of the first three indices equals to zero and the third index is always the negative of the sum of the first two, i= -(h+k). The last hexagonal index refers to the c-direction [23].

Table 2.1: Comparison of the materials properties of Si, 3C-SiC, 4H-SiC, 6H-SiC, GaN and Diamond at 300 K [24].

Material	Si	3C SiC	4H-SiC	6H-SiC	GaN	diamond
Bandgap	1.12	2.36	3.26	3.02	3.39	5.5
Electron mobility, μ_n (cm^2/V.s)	1430	1000 $\perp$ c-axis 1000 $\parallel$ c-axis	1020 $\perp$ c-axis 1200 $\parallel$ c -axis	450 $\perp$ c-axis 100 $\parallel$ c-axis	2000	4500
Hole mobility, μ_p (cm^2/V.s)	600	40	120	80	350	3500
Intrinsic carrier concentration, n_{i} (cm^{-3})	10^{10}	10	10^{-7}	10^{-5}	10^{-10}	10^{-27}
Static dielectric constant, ϵ_s	11.8	9.72	9.76	9.66	8.9	5.5
Thermal conductivity (W/cmK)	1.3	5	5	5	1.3	20
Critical electric field, E_{c} (MV/cm)	0.3	1.4	2.8	3	5	10
Saturation drift velocity (10^5 m/s)	1	2.5	2.7	2	2	2.7
Lattice constant (Å,)	5.43	4.36	c-axis = 10 , a-axis = 3	c-axis = 15, a-axis =3	c-axis = 5, a-axis =3	3.56
Bandgap	Indirect	Indirect	Indirect	Indirect	Direct	Indirect

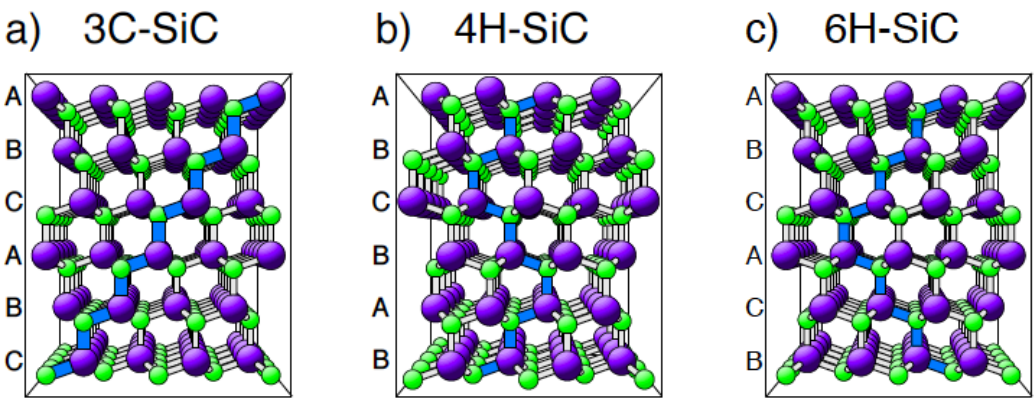


Figure 2.2: The stacking sequences of double layers of a) 3C, (b) 4H and (c) 6H SiC from the side view of $(11\bar{2}0)$ direction. Image taken from [25].

2.3 Future potential of the SiC technology

Nowadays, despite predictions of the physical limitations of silicon, Si-technology continues to dominate in electrical and electronic systems. In the meantime, compound semiconductors have established a good position in those applications where Si technology could not perform well. For an instance, high mobility and direct band structure of III-V semiconductors such as indium phosphide (InP) and gallium arsenide (GaAs) have been extensively employed for light-emitting devices and high-frequency devices [11, 26]. The main competitor for SiC, Gallium Nitride (GaN) has a similar wide bandgap (3.4 eV) and relatively high electron mobility (2000 cm^2/V.s) primarily uses High Electron Mobility Transistor (HEMT) structure for very high frequencies application. However, the process growth for GaN substrates and epi-layer is still in the early stages and much less mature than SiC. On the other hand, the development of SiC devices answers the demands for resilient electronics that can be operated in high temperature, high radiation, high voltage and hostile environments [27]. Potential applications for SiC technology are in the automotive sector, oil and gas drilling sector and nuclear energy generation. The development of gas sensors has created an opportunity for SiC to be utilised as the amplifier, power converter or as the sensor itself [28]. SiC is old but emerging technology. It is also a promising material for power devices due to its superior material properties. As the growth and device-fabrication technology of SiC are advancing day by day, SiC power devices will be widely employed in a wide range of industrial sectors from low to high voltage application areas as shown in Figure 2.3.

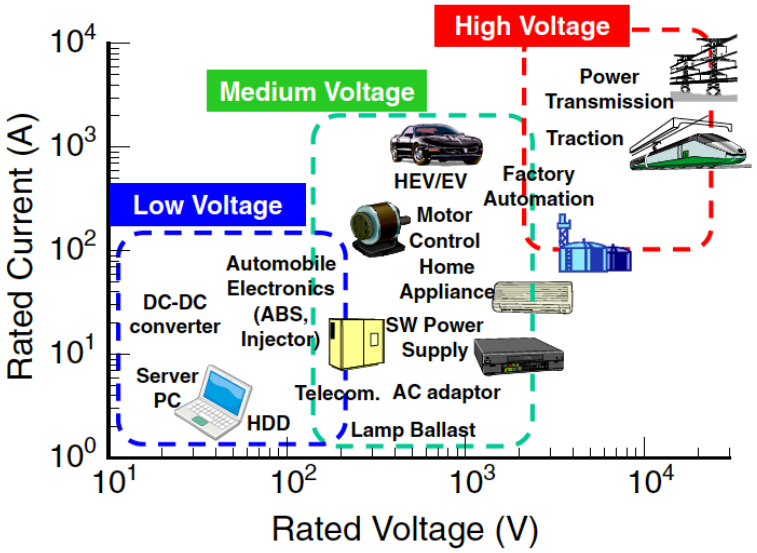


Figure 2.3: Applications area of SiC devices including low, medium and high voltage. Image was taken from [19].

2.4 Key issues and challenges with SiC technology

The potential of 4H-SiC as electronic devices is still in its infancy, despite rigorous research having been performed over the last decades [29]. Key issues and recent developments are now discussed, focusing on the interface state density which is the main issue that limits channel mobility and causes instability in the performance of 4H-SiC MOS devices [30]. Furthermore, current approaches of reducing the interface state density in order to improve the performance of 4H-SiC MOSFETs in term of fabrication process parameters, gate dielectric materials and subsequently a new design will be covered in this section.

2.4.1 Oxidation of 4H-SiC

The ability of SiC to form SiO_2 by thermal oxidation provides a good basis for the fabrication of SiC MOS based electronic devices [31]. Although high-dielectric constant (high-κ) materials such as HfO_2, AIN and Al_2O_3 have been evaluated for 4H-SiC MOSFETs, with a potential to reduce the electric field in the gate dielectric and reduce the threshold voltage, thermal oxidation is still the most commonly use gate dielectric in SiC MOS technology [32].

Due to the stable structure of SiC. This useful characteristic can be utilized in the fabrication of SiC MOS devices. There are few models to clarify the oxidation of SiC, however, it is

different to that of Si and is more complicated due to the presence of carbon. A modified Deal-Grove model was developed for the oxidation of 4H-SiC, which includes the removal of carbon species and the out-diffusion of product gas through the oxide film [33]. In SiC, the oxidation rate strongly depends on the crystal orientation and the oxidation rate of C face is almost one order of magnitude higher than the Si-face.

The reaction of oxidation of SiC can be expressed as

$$\mathrm{SiC} + 1.5\mathrm{O_2} \longrightarrow \mathrm{SiO_2} + \mathrm{CO} \tag{2.1}$$

The formation of the silicon oxide layer at the interface consists of three steps.

1. O_2 molecule approaches the interface through the growing oxide
2. O_2 molecule bonds break apart and forms Si-O-C bonds
3. Carbon is removed from the Si-C bond as a CO molecule

During the oxidation process, carbon atoms in the SiC diffuse out as CO or CO_2. However, there is a small fraction of carbon atoms that diffuse into the bulk forming split interstitial defects [34]. The incomplete CO ejection also causes several type of defects near the SiC/SiO_2 interface, such as carbon interstitials and carbon clusters . Beside carbon related defects, there are also defects at the interface and in the oxide, including Si dangling bonds, Si interstitials and oxygen vacancies[32]. The aforementioned defects are believed to be the origin of the high interface trap density in the bandgap and subsequently result in charge trapping and Coulomb scattering at the interface. Therefore, it is expected that the formation of a thin thermally grown oxide layer will result in the formation of fewer defects and result in a lower interface trap density [35]. Other sources of interface traps that have been suggested as contributing to D_{it} are the oxygen vacancy and oxygen defects [36–38]. In other work [39], the concentration of the life time killer defect (the $Z_{1/2}$ centre, (E_{c}–0.67 eV)) was reduced by thermal oxidation, however, concurrently, other deep level defects such as ON 1 (E_{c}–0.84 eV) and ON 2 (E_{c}–1.1 eV) centers were generated. These defects are thought to be related to both carbon interstitials and the inclusion of N atoms in the SiC. The elimination of $Z_{1/2}$ and $EH_{6/7}$ and the generation of ON1 and ON2 are shown in Figure 2.4, after n-type 4H-SiC samples were oxidized at 1300 °C for 1.3h [40].

In SiC, the value of interface trap density is two orders of magnitude higher than Si at approximately 10^{13} cm^{-2}/eV near the band edges. Electrically active high interface state densities at the SiC/SiO_2 interface are detrimental to the performance of 4H-SiC MOSFETs,

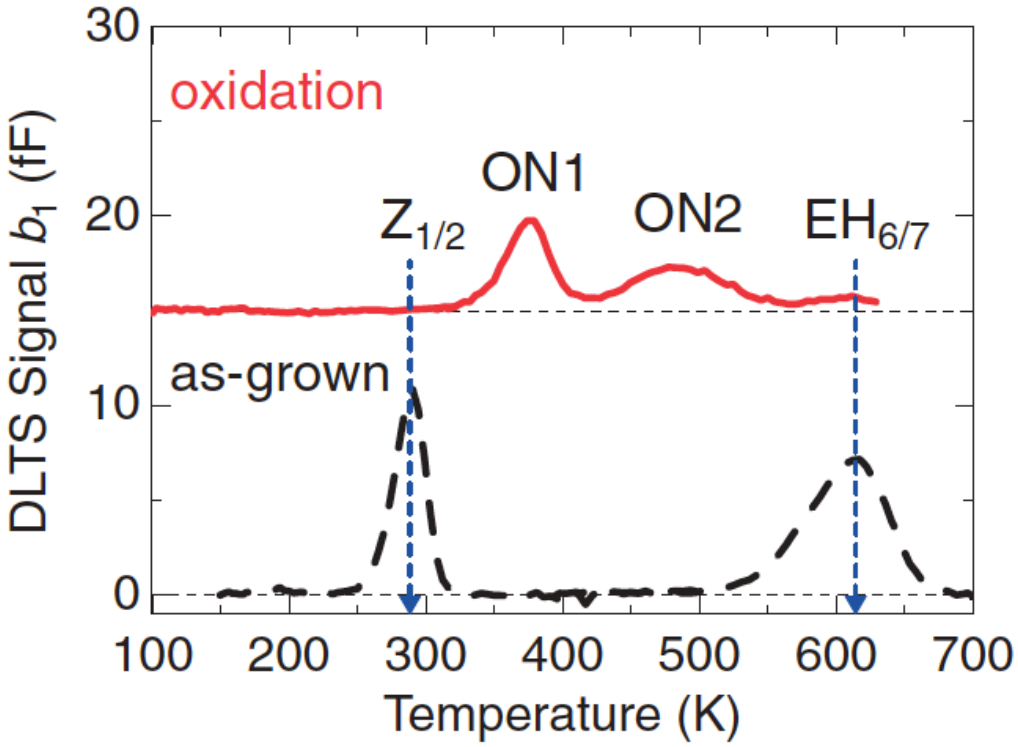


Figure 2.4: DLTS spectra showing the generation of ON1 and ON2 defects after oxidation on n-type 4H-SiC at 1300°C for 1.3h. Image was taken from [40].

since the active area of MOSFETs is at the interface. The interface states trap the free carriers and cause the subthreshold swing, (S) to increase, resulting in a higher threshold voltage. The trapped carriers then act as a charge scattering centre (Coulombic). The scattering rate is directly proportional to the density of occupied interface traps and the fixed charge density at the interface. Hence Conventional lateral 4H-SiC MOSFETs with thermally grown oxide have a typical field effect mobility of approximately 5 cm^2/V.s in comparison to 400 cm^2/V.s for silicon. For this reason SiC will require significant improvements in order to reach the field effect mobility observed in silicon. The low channel mobility can be explained by Coulomb scattering, resulting from the high density of interface traps at the interface. In order to fully realize the potential of SiC MOSFETs, it is necessary to reduce the interface trap density because this will lead to stable device characteristics and better channel mobility.

There are two important challenges to fully utillize the potential of SiC MOSFETs:

1. Increase the channel mobility to $\sim$100 cm^2/V.s
2. Improve the threshold voltage stability at room and high temperature.

These two challenges correspond to greatly improved SiC/SiO_2 interface which is the main

objective in this thesis. Besides interface state density, $D_{\rm it}$, intrinsic defects in the SiO_2 and near interface traps, $N_{\rm it}$ (within 2 nm of the interface) appear to be the dominant factors that degrade electron mobility in the inversion layer [37, 41, 42]. Calculations suggest that silicon interstitials or carbon dimers are responsible for $N_{\rm it}$, however the origin of $N_{\rm it}$ remains unclear.

Sodium can be used to enhance the oxidation rate of SiO_2 and reduce the density of $N_{\rm it}$ [43]. There are two possible explanations as to how sodium suppresses the high density of $N_{\rm it}$.

1) Carbon dimers at the interface are dissolved by the reaction with sodium.

2) Sodium helps carbon atoms that are trapped in the oxide to be transported out through the growing oxide.

While the field effect mobility is impressive, the devices suffer from the threshold voltage instability at typical operating temperatures and gate biases, which makes this method unsuitable for commercial device manufacture.

Phosphorus incorporation has also been reported to effectively reduce $N_{\rm it}$ by reducing the mechanical strain at the SiO_2/SiC interface. The reduced $N_{\rm it}$ results in a high channel mobility up to 89 cm^2/Vs in 4H-SiC MOSFET annealed in phosphoryl chloride $POCl_3$ [41]. On the other hand, Pippel $et\ al.$ have revealed that there is no carbon clusters or graphitic regions at or near the SiO_2/SiC interface, but, instead, $N_{\rm it}$ is caused by the intrinsic defects extending from the interface into the oxide layer. This suggests that $N_{\rm it}$ is an intrinsic defect formed at the SiO_2/SiC interface during gate dielectric formation [37].

2.4.2 Deposited SiO_2

The oxidation of 4H-SiC was reported to create carbon-related defects at the SiC/SiO_2 interface. In particular, it has been suggested that carbon emission towards the bulk of semiconductor occurs during the thermal oxidation, thus affecting the properties of inversion layer [44]. Due to the drawbacks of thermal oxidation, the deposition of SiO_2 using chemical vapor deposition (CVD) or atomic layer deposition (ALD) is an excellent alternative due to the absence of carbon clusters at the SiC/SiO_2 interface and can be deposited at a relatively low temperature ($\sim$300°C). Despite not having a high density or high quality interface between the SiO_2 and the underlying SiC in comparsion to thermally grown oxide, it has been reported that CVD deposited SiO_2 on 4H-SiC combined with high-temperature NO annealing enhanced the channel mobility up to 27.7 cm^2/V.s [45]. ALD SiO_2 on 4H-SiC with N_2O post-deposition

annealing at 1100°C exhibited peak field effect mobility of 25.9 cm^2/V.s with a threshold voltage of 4.6 V [46]. A thin SiN buffer layer on the Si-face of 4H-SiC followed by SiO_2 deposition and N_2O annealing has been reported to increase the field-effect mobility to above 30 cm^2/V.s in lateral n-channel MOSFETs [47]. The benefits of deposited SiO_2 in the improvement of field effect mobility and threshold voltage stability in comparison to thermally oxide MOSFET has voided the advantages of thermal oxide SiO_2.

2.4.3 Post oxide annealing

Comprehensive research has been performed to improve the quality of the SiC/SiO_2 interface that is believed to be the origin for the degradation of channel mobility either due to trapped or scattered carriers. Thermally grown SiO_2 SiC MOSFETs exhibit extremely low values of field effect mobility as low as 10 cm^2/V.s due to the high density of interface states, $D_{\rm it}$ [48]. While hydrogen annealing efficiently reduces the interface state density at silicon interface, its impact at SiC interfaces is significantly reduced [49]. The most common technique that has become a standard process to produce commercial quality devices with channel mobility about 30 cm^2/V.s is post oxidation annealing (POA) of the gate oxide using nitrogen rich atmosphere, typically nitric oxide (NO), nitrous oxide (N_2O) or nitrogen (N_2), that is also known as nitridation or passivation.

Nitridation

It has been shown that nitridation improves the MOS interface quality and decreases the interface density, resulting in a 5 fold increase in field effect mobility in comparison to un-annealed MOSFET [32, 50]. The higher channel mobility is coupled with a lower threshold voltage, which can be achieved by increasing the annealing temperature.

At high temperatures above 1000°C, N_2O molecules decompose to form a nitrogen molecule and a free oxygen atom. The oxygen atom could turn to oxygen molecule or reacts with the nitrogen to become NO. Therefore, during N_2O annealing, both oxidation and nitridation of the SiC takes place and results in a slightly thicker oxide in comparison to NO annealing. Since dry oxidation produces a high density of interface traps, NO annealing is an effective technique to suppress the interface state density, $D_{\rm it}$. MOSFETs with NO-annealed oxides give higher channel mobilities than those with N_2O-annealed oxides on both the Si (0001) and C ($000\bar{1}$) faces of SiC. MOSFETs on the ($11\bar{2}0$) face exhibited significantly higher channel mobility ($>$ 100 cm^2/V.s) than those on (0001) and ($000\bar{1}$), irrespective of any nitridation process [50].

It is known that NO or N_2O nitridation has two functions [50–52]: (1) creating strong Si-N bonds for passivating dangling Si bonds and replacing strained SiO bonds, and (2) removing carbon atoms or clusters accumulated during oxidation by CO or CO_2 out-diffusion [53]. The reduced density of residual carbon atoms or clusters at the near or at the interface leads to an improved SiO_2/SiC interface with low interface-state density [54]

Scanning spreading resistance microscopy (SSRM) has been performed to measure the resistance of the surface channel region [55]. It was suggested that nitrogen atoms incorporated at the interface and substrate resulted in an increase in the conductivity of MOSFET channel. X-ray photoelectron spectroscopy (XPS) measurements were used to detect the density of nitrogen atoms at the SiC surface. A high density of nitrogen atoms (10^{14} cm^{-3}) was observed to be accumulated at the SiC/SiO_2 interface for samples that were annealed in NO ambient at 1200°C [56]

Phosphorus

Despite the excellent reduction of $D_{\rm it}$ by means of a nitridation process, the channel mobility of 4H-SiC is still far lower than theoretical expectations [52, 57]. The idea of incorporation of other atoms in the same group (phosphorus) was proposed by Okamoto $et\ al.$ [2]. It was found that the interface state density near the conduction band edge can be significantly reduced with $POCl_3$ annealing, resulting in an improvement in the channel mobility to 89 cm^2/V.s [41]. A high concentration of uniformly distributed P atoms was observed at the interface using secondary ion mass spectroscopy. P atoms do not diffuse into the SiC, due to the small diffusion coefficient. It was suggested that the strain at the SiC/SiO_2 interface is relaxed by the incorporation of P atoms. As the result, the channel mobility increases significantly. Low interface trap density and high channel mobility of 125 cm^2/V.s was reported on $(11\bar{2}0)$ a-face 4H-SiC [58], however the incorporation of phosphorus in the oxide of n-channel results in threshold voltage instability. The data suggest that the oxide traps in phosphorus doped oxides are the main contributor to this problem [59]. The threshold voltage stability can be improved by reducing the thickness of the phosphorus doped SiO_2 to approximately 10 nm [60] and increasing the phosphorus concentration [61], but further optimization of the fabrication process is still ongoing [42].

Boron

Recently, improvements in channel mobility with a peak field-effect mobility of 102 cm^2/V.s was successfully demonstrated on a (0001) Si-face using boron passivation [62]. Boron nitride (BN) was used as a planar diffusion source. As with P, B is incorporated at the SiC/SiO_2

interface dramatically reducing $D_{\rm it}$ and increasing the channel mobilty, but this cannot be explained by counter doping effects because B atoms act as an acceptor (boron is in group III in periodic table). A study using Fourier transform infrared absorbtion and XPS showed that B atoms at the interface relax the stress in the oxide network close to the interface [62, 63]. Furthermore, the presence of both nitrogen and boron atoms during the oxide formation results in an enhanced field effect mobility up to 160 cm^2/V.s [63]. The incorporation of B atoms in nitrided oxide has given significant improvement in threshold voltage stability under both positive and negative bias stress and high temperature in comparison to undoped nitrided MOSFET structures. Antimony counter doping combined with a borosilicate glass (BSG) gate dielectric process resulted in a MOSFET with the highest field effect mobility-threshold voltage (μ-$V_{\rm TH}$) product recorded to date [64]. A maximum peak of field effect mobility of 180 cm^2/V.s with tunable threshold voltage from 2.5 to 0.9 V was succesfully fabricated. However, the poor performance of the bias temperature instability still remained as a big issue for the devices fabricated using this process.

Pyrogenic/Hydro-treatment

Kikuchi $et\ al.$ fabricated SiO_2/4H-SiC (0001) metal-oxide-semiconductor capacitors by thermal oxidation at 1300°C in a ramp-heating furnace with a short rise/fall time, followed by low temperature O_2 anneal at 800°C. Based on thermodynamic and kinetic considerations of the SiC oxidation process, the thermal oxidation conditions were optimized and nearly ideal capacitance-voltage characteristics were obtained [35]. In 2004, the effect of pyrogenic gate oxidation (H_2O atmosphere containing O_2) and pyrogenic gate oxidation followed by H_2 post-oxidation annealing (POA) on 4H-SiC was investigated [65, 66]. The results suggested that the presence of H or OH dramatically decreased the $D_{\rm it}$ and the threshold voltage markedly improving field effect mobility, $\mu_{\rm FE}$ to 111 cm^2/V.s [65]. The effect of pyrogenic or hydrotreatment processes depends on the crystal face, being effective on the C-face but not on the Si-face [67, 68]. The explanation behind this is still remain unclear.

Enhanced oxidation (sodium/ barium)

The incorporation of sodium during the oxidation process increases the oxidation rate and suppresses the formation of interface traps, resulting in a high inversion channel mobility of up to 150 cm^2/V.s [43]. The sodium is incorporated by using carrier boats made of sintered alumina during oxidation or by deliberate sodium contamination of the SiC prior to oxidation. It has been suggested that sodium impurities are responsible for accelerating the oxidation rate by increasing the permeation of oxygen through the growing oxide [69]. Another possible

explanation for this is that sodium acts as a carrier to transport carbon out of the growing oxide [43]. However, the underlying mechanism for the reduction of interface trap is still unclear and this technique results in significant V_{TH} instability due to the presence of mobile charge, hence, it isn't considered to be suitable for commercial devices. The use of barium (an alkaline earth element) as an interfacial layer between SiC and the gate oxide has resulted in high field effect mobility of approximately 85 cm^2/V.s significantly higher than that obtained with alkaline earth elements including Ca and Sr [70]. Different Ba source materials such as $BaCO_3$ and $BaNO_3$ have been reported to produce different peak mobility (from 70 to 100 cm^2/V.s) depending on the device fabrication process. Similar to sodium, barium also enhances the oxidation rate of not only SiC [71, 72] but also Si [73].

The data in table 2.2 summarises the important parameters of the fabricated MOSFETs including threshold voltage, oxide breakdown field, device dimension (length $\times$ width) and peak field effect mobility for n-channel MOSFETs with different gate dielectric formation using data taken from the literature data.

2.4.4 Recent advances in higk-κ dielectric technology for SiC MOSFET

In order to operate SiC devices under extreme conditions, it is necessary to find suitable dielectric materials to passivate the surface of the device to avoid excessive leakage and early breakdown. Since SiO_2 can be grown by thermal oxidation, it has been used as a passivation (gate dielectric) between metal gate contacts and SiC for many years. SiO_2 has a dielectric constant that is 2.5 times lower than that of SiC and poorer SiO_2/SiC interface properties [82] in comparison to the SiO_2/Si interface. This reduces the maximum surface field in the SiC to avoid SiO_2 breakdown and this significantly limits the extraordinary abilities of SiC. This large electric field in the dielectric in comparison to that in the semiconductor is the driving force behind research into new dielectrics with a dielectric constant at least similar to that of SiC and lower interface states densities are desired for device applications [83, 84]. In order to obtain the ultimate performance from SiC, it is important to find new dielectric materials that are compatible with SiC that meet the requirements below:

1. high dielectric constant and large bandgap in comparison to SiO_2
2. high band offset with electrodes and SiC
3. thermally and chemically stable in contact with semiconductor substrate

Table 2.2: Summary of important parameters for n-channel SiC MOSFET with different gate dielectric formation.

Ref	V_{TH} (V) / E_{BD} (MV/cm)	gate dielectric treatment	device size L × W (μm)	peak field effect mobility (cm^2/V.s)
[74]	6.8 / 9.2	oxidation of thin Silicon Nitride + PECVD SiO_2	40 × 250	18.6
[75]	3 / -	4H-SiC(0-33-8) face	100 × -	80
[76]	0.46 / -	POA in N_2O at 1150°C	10 × 100	42
[77]	1 / -	N_2O and N_2 anneling of deposited Si_2 TEOS	4 × 150	12
[78]	2.4 / -	nitrogen implantation	650 × 80	21.9
[79]	1 to 1.2 / -	Antimony counter doping	150 × 290	80-110
[2, 41]	0 / 9.5	POA using phosphoryl chloride ($POCl_3$)	30 × 200	89
[4, 60]	0.5 / 8	phosphorus planar diffusion source (PDS)	150 × 290	80
[61]	1 / -	different annealing temperature 900 to 1100°C in ($POCl_3$)	150 × 290	105
[58]	3.6 / -	phosphorus and nitrogen passivation on $(11\bar{2}0)$	150 × 290	125
[62]	1.3 / -	BN planar diffusion source	100 × 150	102
[63]	2 / -	oxynitrided gate oxide + BSG diffusion	25 × 150	160
[64]	0.9 to 2.5 / -	Antimony counter doping + BSG diffusion	200 × 200	180
[65]	1.4 / -	H_2O atmosphere containing O_2 pyrogenic gate oxidation + H_2	100 × 150	111
[66]	3.1 / -	Hydrogen POA on $(11\bar{2}0)$	100 × 150	110
[43, 80, 81]	4 / 8-10	oxidation in alumina environment	100 × 200	170
[70, 71]	-1 / 10	using alkali and alkaline earth interface layers	200 × 200	85

4. compatibility with gate electrode material

5. low lattice mismatch and similar thermal expansion coefficient with SiC

6. negligible capacitance-voltage hysteresis (< 20 mV)

7. good long term reliability

In the last decade, significant progress has been reported in the processing of dielectrics for SiC MOSFET fabrication. A number of potential high-κ dielectric materials such as Al_2O_3 [85], hafnium dioxide (HfO_2) [86–88] and lanthanum silicate ($LaSiO_x$) [89, 90] have been explored as components for gate stacks in order to improve the channel mobility. Lanthanum oxide, La_2O_3, is one of a potential high-κ to use as an interfacial layer between SiC and SiO_2. During high temperature annealing, La_2O_3 turns into $LaSiO_x$ and acts as an interfacial layer, resulting in the reduction of $D_{\rm it}$ [89]. High peak channel mobility of 133.5 cm^2/V.s with positive threshold voltage (3 V) was reported after 900°C post-deposition annealing (PDA) in N_2O [91]. This study has shown that the formation of an ultra thin La-silicate layer in conjunction with ALD SiO_2 is a promising route to increase the field effect mobility, while also achieving a positive threshold voltage. However, the bandgap of La_2O_3 is relatively small (4.3 eV) in comparison to other high-κ materials such as Al_2O_3 (6.2 eV) and HfO_2 (5.4 eV). A narrow bandgap results in smaller barrier height or energy band offsets with SiC and thus results in a significant increase in the oxide leakage current [92]. A band offset less than 1.0 eV may lead to an unacceptably large leakage current and ideally the bandgap of the gate dielectric should be at least 7 eV [82].

The potential of silicon nitride / silicon oxide, (SiN_x/SiO_2) stack-gate structures deposited by PECVD has been explored [93]. Interestingly, Metal-oxide-semiconductor field effect transistor (MISFETs) fabricated with a SiN_x/SiO_2 layer of 2 nm / 50 nm annealed in N_2O for 5 min demonstrated a relatively high channel mobility of 32 cm^2/V.s on the (0001)Si face and 40 cm^2/V.s on the $(000\bar{1})$ C face. However, these devices showed a large negative shift in threshold voltage at high temperatures due to the presence of positive charges in the SiN_x layer. Nevertheless, the effect of negative shift in threshold voltage can be suppressed by reducing the SiN_x thickness.

MOCVD-grown Al_2O_3 has been investigated as the gate dielectric for 4H-SiC MOSFETs [94]. A high field-effect mobility of 64 cm^2/V.s was reported for the Al_2O_3 film deposited at 190°C. A significant increase in the channel mobility to 300 cm^2/V.s was achieved by incorporating an interfacial layer of SiO_2 layer (less than 1.3 nm) between the Al_2O_3 and the SiC. It

Table 2.3: Summary of potential high-k material.

Material	κ value	bandgap (eV)
SiO_2	3.9	9
Al_2O_3	9	8.8
HfO_2	15-25	5.7
La_2O_3	21	6
ZrO_2	15-25	5.7

was suggested that the thickness of the SiO_2 layer plays an important role in supressing the Coulomb scattering in the channel [94]. Nevertheless, the stability of the device characteristics is poor, especially at high temperatures, due to the negative charge trapping effect in the Al_2O_3 [95, 96]. Table 2.3 summarizes the dielectric constant (κ value) and bandgap of commonly investigated high-κ materials. Note that the values for high-κ and bandgap depends on the fabrication process.

2.4.5 High-κ dielectric; aluminium oxide, Al_2O_3

The need for highly reliable dielectric films for SiC devices has become increasingly urgent to enable their deployment in hostile environments, such as those found in aerospace and oil and gas exploration. SiO_2 is the most popular gate dielectric owing to its superlative material properties [34, 97, 98]. Nitridation of $SiO_2$2/SiC interface using nitrogen oxide (NO) increases the field effect mobility, but as the mobility increases the threshold voltage of the device reduces, eventually becoming negative for very high mobilities [99]. The dielectric constant of SiO_2 (3.9), is low in comparison to that of SiC, resulting in a high electric field in the SiO_2 for devices operating at high voltages. Therefore, a new highly reliable dielectric with a permittivity similar to that of SiC is desired. A range of dielectrics including HfO_2, aluminium oxide (Al_2O_3) and lanthanum oxide (La_2O_3) have been investigated in terms of performance and reliability [100]. Al_2O_3 is a potential high-κ material with conductance and valence band offsets of 1.7 eV and 1.2 eV respectively, sufficient to prevent electron and hole injection into the dielectric [101]. The band offset of Al_2O_3/SiC can be further increased by the deposition of a thin layer of SiO_2 prior to Al_2O_3 deposition [102].

High channel mobility in 4H-SiC MOSFETs with Al_2O_3 gate dielectric has been previously demonstrated [94, 103]. The interfacial properties of Al_2O_3/SiO_2/SiC was reported to be better

than Al_2O_3/SiC in terms of reduced leakage current and interface state density, $D_{\rm it}$ [96]. It has been reported that post oxidation annealing (POA) of Al_2O_3 in H_2 at 500°C reduced $D_{\rm it}$ to the level of 10^{11} cm^{-2}/eV in the mid-gap of 6H-SiC. However, due to significant charge trapping in the oxide and at the interfaces, significant hysteresis in the capacitance–voltage (C-V) characteristics and deviation in flatband voltage with different bias voltages was observed [96, 104]. More recently reports indicate that post deposition hydrogen treatment is a promising technique for the reduction of $D_{\rm it}$ at the 4H-SiC/Al_2O_3 interface; however the stability of C-V characteristics remains to be determined.

Table 2.4 summarizes the important parameters, including threshold voltage and peak field effect mobility from SiC MOS capacitors / MOSFET utilizing Al_2O_3 as a gate dielectric. There are a number of process techniques that can be used to deposit an Al_2O_3 layer. The most commonly used technique is ALD. ALD is a self-limitng and sequential growth process using reactive precursors trimethylaluminum (TMA) and H_2O or oxygen. This technique offers high conformality on any kind of surface profile with precise control of composition and thickness down to the nanoscale and requires relatively low growth temperatures (200-300°C). For these reasons, this technique is ideal for samples with complex surface and low temperature budget applications. As shown by the data in the Table 2.4, the highest reported peak field effect mobility for SiC MOSFET utilizing Al_2O_3 as a gate dielectric is around 300 cm^2/V.s. The MOSFET was fabricated with an ultrathin (sub 1nm) thermally grown SiO_x layer between the Al_2O_3 and the SiC. The increase in mobility is due to the presence of the thin layer SiO_x that acts as a barrier layer against the diffusion of radical species produced during Al_2O_3 deposition [105]. The lower strain at the Al_2O_3/SiO_x/SiC interface in comparison to the SiO_2/SiC interface is thought to contribute to the low interface state density [106]. However, the reliability and the stability due to negative charge trapping effects in Al_2O_3 still require investigation.

Deposition of Al_2O_3

Al_2O_3 can be prepared by subsequent repetition chemical reaction of trimethylaluminum $Al(CH_3)_3$ and H_2O [107]

$$2\mathrm{Al(CH_3)_3} + 3\mathrm{H_2O} \rightarrow \mathrm{Al_2O_3} + 6\mathrm{CH_4} \tag{2.2}$$

Deposition conditions typically range between 200°C to 300°C, where the substrate temperature does not affect the growth rate, for pressures in the range 1 to 10 hpa (mbar). The deposition pressure can be controlled with inert carrier gas (N_2). Firstly, the metal precursor

Table 2.4: Summary of important parameters of SiC MOSFET utilizing Al_2O_3 as a gate dielectric.

Ref	V_{TH} (V)	gate dielectric treatment	device size (L × W (μm)	peak field effect mobility (cm^2/V.s)
[94, 102]	2.8	ultrathin layer of SiO_2 + MOCVD Al_2O_3	10 × 100	300
[94, 102]	3.2	MOCVD Al_2O_3	10 × 100	64
[95, 103]	0.8	1175°C NO anneal (SiO_2) + Al_2O_3	200 × 400	106
[95, 103]	1.4	1000°C NO anneal (SiO_2) + Al_2O_3	200 × 400	62
[104]	-	hydrogen plasma pretreatment + annealing in forming gas	–	57

TMA is pulsed to the reaction space. The trimethylaluminum $Al(CH_3)_3$ molecules react with the -OH groups on the substrate surface. Then, surplus TMA molecules and methane (CH_4) molecules are released from surface reactions by purging the reaction space with inert gas (Fig 2.5).

Subsequently, H_2O is pulsed into the reaction space as in Fig 2.6 and reacts with the TMA molecule fragments attached to the substrate surface. Again, the chamber is purged with inert gas. The growth of a thin film is achieved by repeating this pulse and purge cycle until the desired thickness is obtained. Typically, one cycle results in a dielectric thickness of 1Å

Advantages of ALD

ALD is well known for its capability of producing excellent film uniformity on any type of substrates. It has a unique step film coverage compared to other deposition techniques, such as PECVD and PVD where it has the ability to control film thickness due to self limiting growth mechanism [109]. Fig 2.7 show a typical coverage of 300 nm amorphous aluminium oxide, Al_2O_3 on trench structure of silicon.

Since ALD has become a technique for the deposition of metals, metal nitrides and dielectrics, it has received a lot of attention. Currently, a wide range of film materials are currently available as precursors. Another advantage of ALD is the lower deposition temperature in comparison

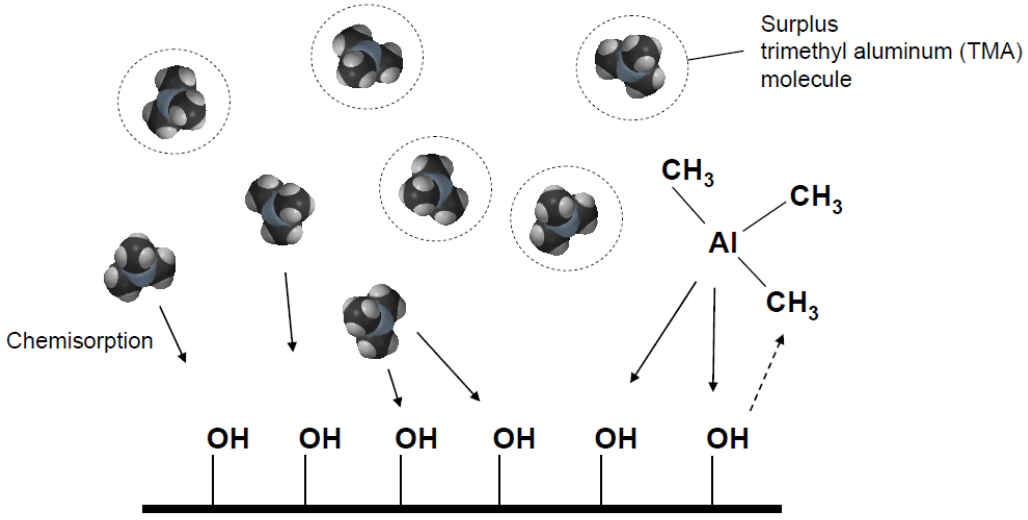


Figure 2.5: TMA molecules reating with the -OH groups on the substrate.

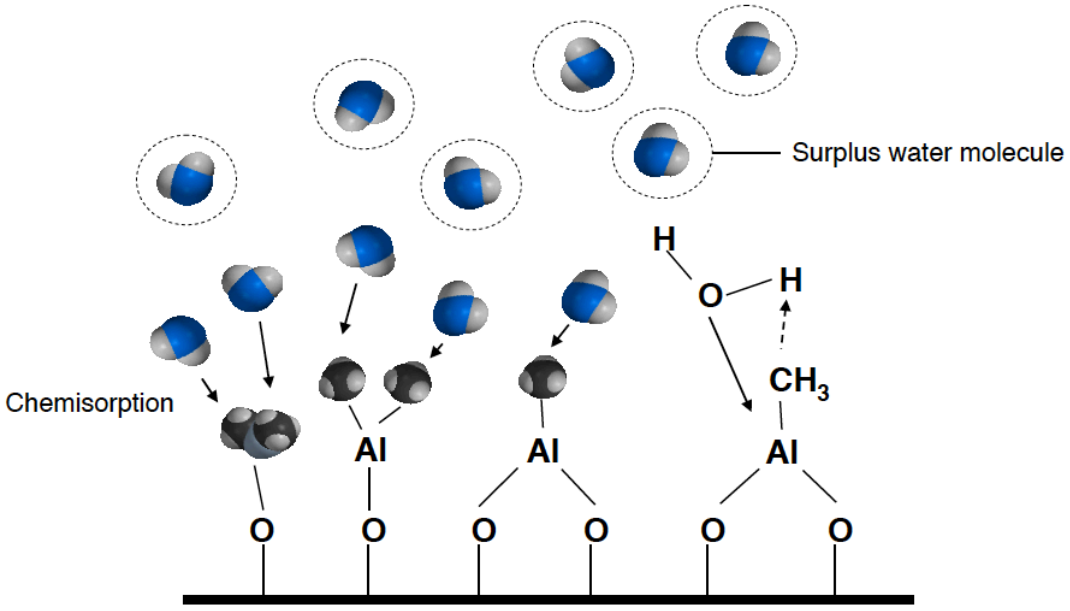


Figure 2.6: H_2O molecules react with the TMA molecule fragments attached to the substrate surface.

to CVD technique, enabling it to be used for sensitive substrates that need low temperature process.

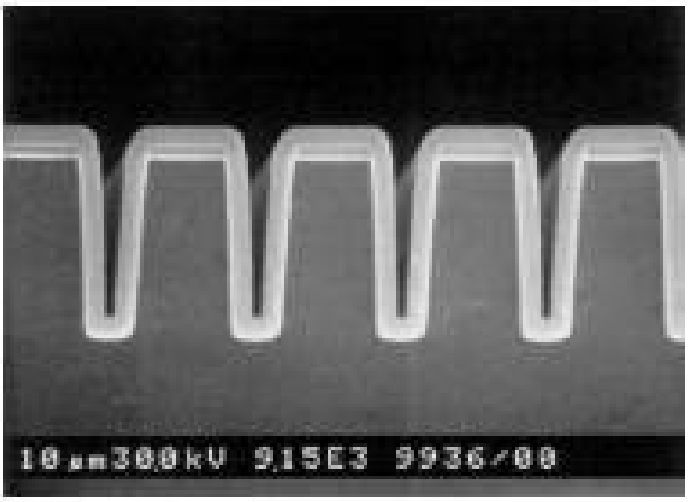


Figure 2.7: Cross section TEM image of 300 nm Al_2O_3 deposited by ALD on trench structure of silicon. Image was taken from [108]. No scale was provided from the literature.

2.4.6 Interface state density

The interface traps in silicon MOS systems are formed because of an excess of oxygen or silicon and dangling bonds of Si at the interface. Forming gas annealing has been shown to effectively reduce the density of traps at the Si/SiO_2 interface. It is known that the density of traps present near the band edge of 4H-SiC/SiO_2 is high (10^{13} cm^{-2}/eV) in comparison to the Si/SiO_2 interface [110, 111]. The origin of these traps are attributed to the imperfect surface of 4H-SiC, dangling bonds of Si and C and carbon clusters that trap free carriers at the interface, increasing the resistance in the channel region. However, it was found that the channel mobility for 4H-SiC is lower than 6H-SiC which is unexpected because 4H-SiC has higher bulk mobility. According to Schorner $et\ al.$ [112], the interface state density is fixed at approximately 2.8 to 3 eV above the valence band edge. As can be seen in Fig 2.8 (a), since 6H-SiC has energy bandgap of 3 eV, the majority of the defect states are located in the conduction band, thus do not effect the channel mobility in the inversion layer. In 4H-SiC, the defect states lie with in the forbidden bandgap or at the edge of 4H-SiC bandgap. Hence, the channel mobility in 4H-SiC is reduced by the trap and Coulomb scattering effect.

Fig 2.8 (b) shows the location of the defect states system at the interface between the oxide and the semiconductor. In general, interface traps that are located within the bandgap can be either acceptor-like or donor-like [113]. Donor-like traps are positively charged when empty and neutral when occupied by electrons. The acceptor-like traps that are located between

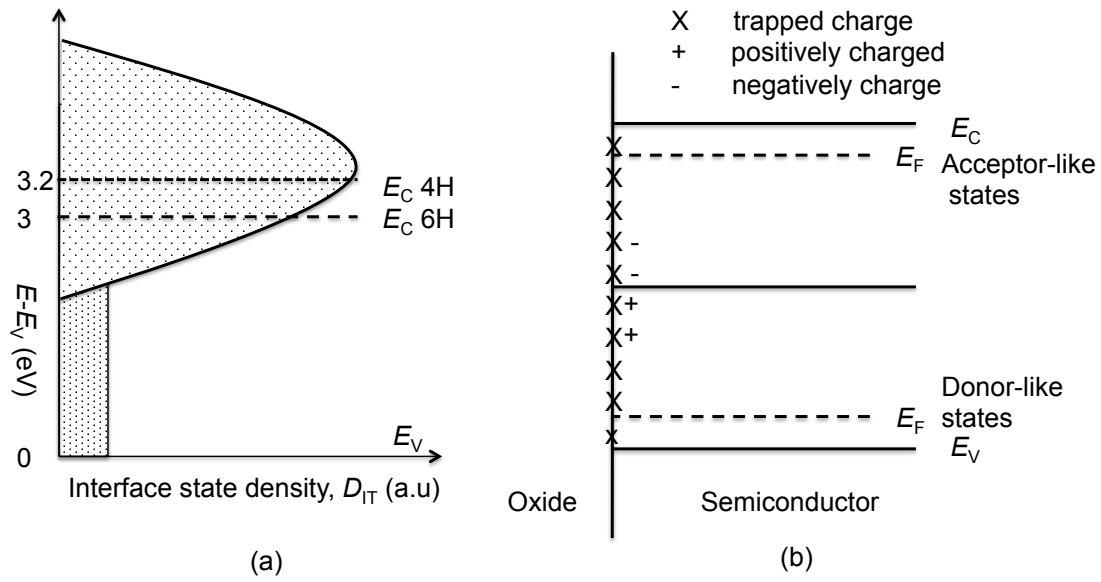


Figure 2.8: (a) Illustration of the distribution of interface state density within the bandgap of 4H-SiC and 6H-SiC. (b) Interface states system at oxide/semiconductor interface including donor-like and acceptor-like state with in bandgap.

the mid gap and conduction band edge are neutral when empty and negatively charged when occupied by electrons. The C-V curve shifts towards the negative voltage when the interface state charge is positive and shifts towards the positive voltages when the interface state charge is negative. For p-type semiconductors, the traps are primarily donor-like and are located between the mid-gap and valence band. P-type SiC MOS capacitors commonly demonstrate large negative flatband voltage due to the positive interface state charge, which results in a decrease in the minority carrier density (electrons) to fill the states [112]. Similarly, for n-type semiconductors, the traps are primarily acceptor-like and are located between the mid-gap and conduction band. N-type SiC MOS capacitors commonly demonstrate positive flatband voltage due to the negative interface state charge.

2.5 The MOS capacitor

2.5.1 MOS Fundamentals

The metal–oxide–semiconductor system is the critical component of the MOS field effect transistor (MOSFET). To study MOSFETs under manufacturing conditions, the MOS capacitor has been used extensively as a test structure. The MOS capacitor has the advantages of simplicity in fabrication and analysis. Fabrication of the MOS capacitor uses the same

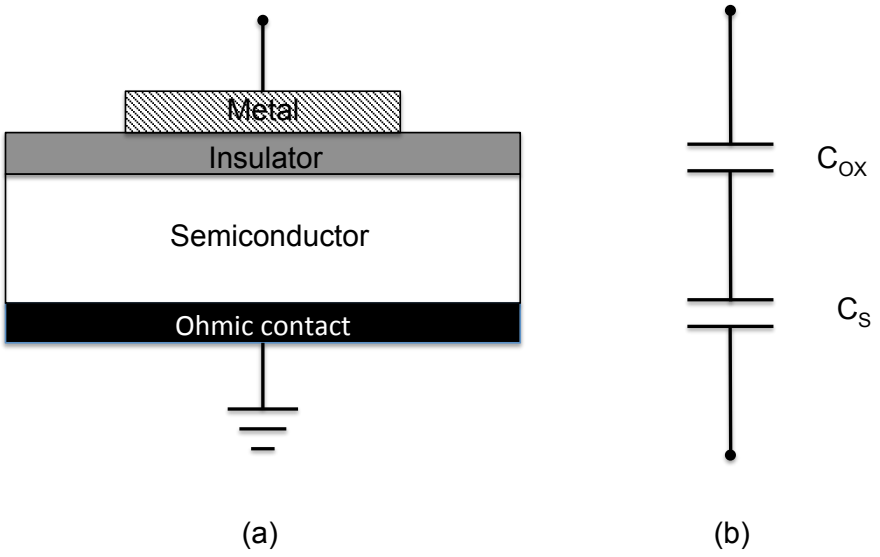


Figure 2.9: Schematic cross-section of an (a) Ideal Metal-Insulator-Semiconductor (MIS) capacitor and (b) the equilvalent circuit.

processing used for the MOSFET, therefore, the MOS capacitor provides direct measurement and monitoring of the MOS system. The basic concepts of MOS capacitors and MOSFETs will be discussed in this section.

2.5.2 MOS capacitor

A MOS capacitor consists of a gate metal (metal or heavily doped polysilicon), gate dielectric and semiconductor substrate (n-type or p-type). The structure of a MOS capacitor is shown schematically in Figure 2.9 (a). The MOS capacitor behaves as two capacitors (oxide capacitance, C_{OX} and semiconductor capacitance, C_{s}) connected in series, as illustrated by the equivalent circuit in Figure 2.9 (b). The diagram in Figure 2.10 illustrates the energy band diagram of MOS capacitor under equilibrium flatband conditions, where E_0 represents the vacuum level which is the minimum energy that electron requires to leave the surface. E_F is the Fermi energy of the semiconductor, E_C the conduction band and E_V the valence band. The energy difference between E_0 and E_F is defined as $q\Phi_M$, the metal work function. E_i is the intrinsic energy level of the semiconductor (temperature dependent) and Φ_B the bulk potential or the energy different between Fermi energy and intrinsic energy of semiconductor [114].

The shape of a C-V curve depends on the measurement frequency and the type of semiconductor. The C-V curve has 3 important regions: accumulation, depletion and inversion.

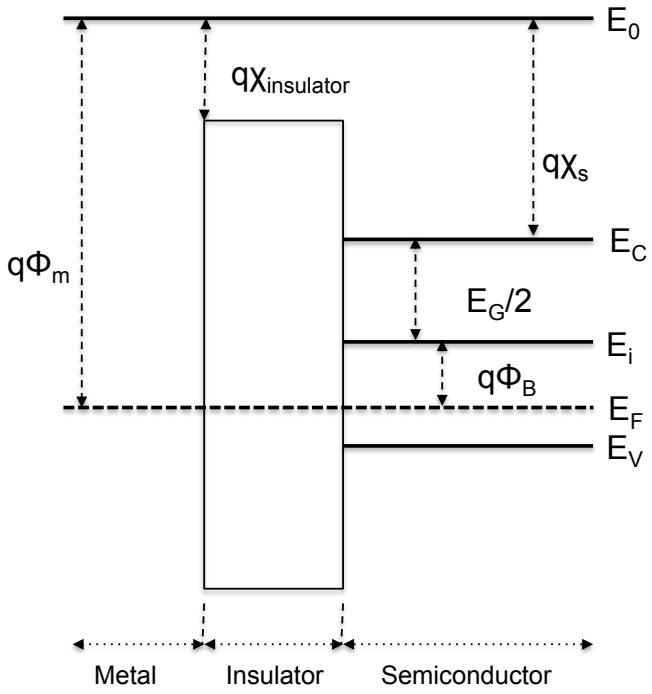


Figure 2.10: Schematic of ideal MOS capacitor energy band diagram under equillibrium conditions.

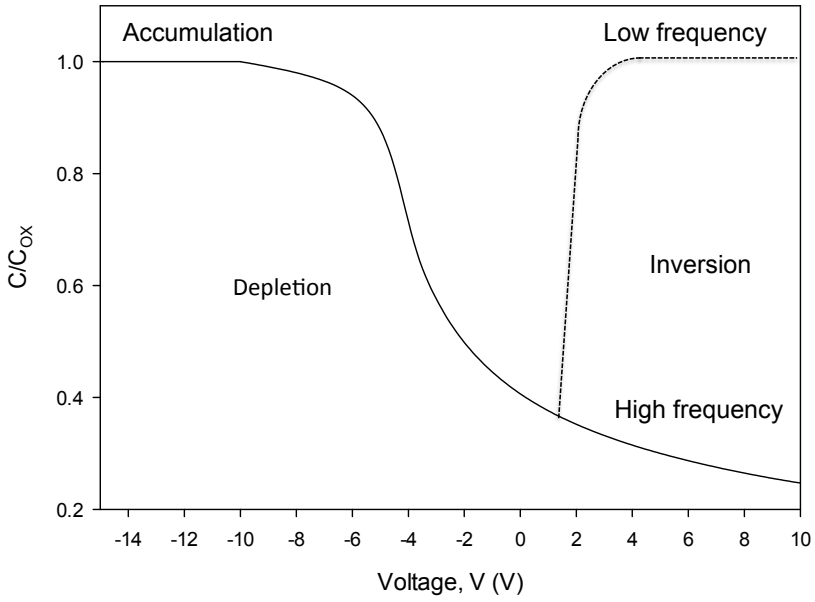


Figure 2.11: Normalized C-V curve for p-type MOS capacitor with different type of frequencies.

Figure 2.11 schematically illustrates a C-V curve for a p-type MOS, where the applied potential is with respect to the grounded substrate. For an n-type MOS, the C-V response is similar but the curve is a mirror image of p-type MOS, where the majority carriers are electrons.

Flatband voltage

As shown in Fig 2.10, at zero applied bias, the energy band is aligned to the Fermi level, E_F of the gate and semiconductor. Ideally, it is determined by the difference in the work function of metal and semiconductor. The band bending changes with the applied voltage and it is called the flatband voltage when the bands in the bulk of the semiconductor become flat.

Accumulation

Accumulation is the region of the C-V curve when a large negative voltage is applied to the gate contact ($<V_{\mathrm{FB}}$). The negative bias raises the Fermi level of the metal with respect to E_0 and results in the bands bending upward (refer Fig 2.12 (a)). The Fermi level at the oxide/semiconductor interface is close to the semiconductor valence band in comparison to intrinsic energy level. The negative charge/polarity attracts holes (majority carrier in p-type MOS) to the gate and this excess charge forms an accumulation layer. However, since the oxide acts as an insulator, the holes do not flow to the gate and instead accumulate at the oxide/ semiconductor interface. The measured capacitance is therefore based dominantly on the capacitance of the gate dielectric (assuming that the capacitance of the accumulation is very large).

Depletion

As the voltage becomes more positive, the positive gate repels the majority carriers (holes) into the semiconductor and creates a depletion region until it reaches a maximum depletion width, $W_{\max}$. The positive bias of the gate lowers the Fermi level of the metal gate. The valence band at the interface is now further away from the the Fermi level, lowering the hole concentration ((refer Fig 2.12 (b)). The total capacitance in the depletion region is a series combination of C_{OX} and C_{s}. However, SiC MOS capacitor exhibits deep depletion due to the wide bandgap and low intrinsic carrier concentration (10^{-7} cm^{-3} at the room temperature). Here the minority carriers do not follow the ac gate voltage, hence, do not contribute to the capacitance. In particular, the depletion width continues to increase with gate bias until oxide breakdown occurs. This a problem for SiC MOS devices because the minority carriers are required to form the channel between source and drain (MOSFET)

From the equivalent circuit shown in Figure 2.9 (b), the total capacitance density, C_{T}, can be expressed as,

$$1/C_{\mathrm{T}} = 1/C_{\mathrm{OX}} + 1/C_{\mathrm{s}} \tag{2.3}$$

The depletion width can be calculated from

$$W_{\mathrm{dep}} = \sqrt{\frac{2\varepsilon_{\mathrm{SiC}}\varepsilon_0\psi_S}{qN_{\mathrm{A}}}} \tag{2.4}$$

where $\varepsilon_{\mathrm{SiC}}$ is the semiconductor relative permittivity, q the electron charge and N_{A} the acceptor concentration. The depletion charge per unit area may be expressed as

$$Q_{\mathrm{dep}} = qN_{\mathrm{A}}W_{\mathrm{dep}} \tag{2.5}$$

Inversion

At positive bias, when the growth of the depletion region is restricted, the density of the minority carriers (electrons) increases at the interface and form an inversion layer that has an equivalent concentration to the acceptor concentration in the semiconductor (n_{s} = N_{A}). In the band diagram, the band bends downward, so that the conduction band approaches the Fermi level, resulting in a high electron concentration at the interface (refer Fig 2.12 (c)). The total capacitance in the inversion region depends on the frequency of the applied voltage. The frequency dependence of inversion capacitance is related to the minority carrier response time. Minority carrier follows an applied ac gate voltage if the period of the applied ac voltage is longer than the minority carrier response time. At high frequency, the ac probe is too high for the inversion charge (minority carriers) to be able to respond, but as the frequency reduces, the ac probe is able to get the respond of the minority carriers and results in an increase in the measured capacitance.

In the context of energy conservation, V_{G} can be expressed as,

$$V_{\mathrm{G}} = V_{\mathrm{FB}} + V_{\mathrm{OX}} + \psi_{\mathrm{S}} = V_{\mathrm{FB}} + \frac{Q_{\mathrm{S}}}{C_{\mathrm{OX}}} + \psi_{\mathrm{S}} \tag{2.6}$$

where V_{OX} is the voltage across the oxide, ψ_{S} the surface potential, Q_{S} the total surface charge at the interface and C_{OX} the oxide capacitance.

The surface potential at the point of strong inversion is twice that of the bulk potential and can be expressed as

$$\psi_{\mathrm{S}} = 2\psi_{\mathrm{b}} = 2\frac{kT}{q}\ln\left(\frac{N_{\mathrm{A}}}{n_{\mathrm{i}}}\right) \tag{2.7}$$

where the bulk potential can be expressed as ψ_{b}=($E_{\mathrm{F}} - E_{\mathrm{i}}$)/$q$. Where n_{i} is the intrinsic carrier concentration, k is Boltzmann's constant and T the absolute temperature.

In the inversion regime, the depletion region is the maximum width, $W_{\max}$. It can be expressed by substituting Eq 2.7 into Eq 2.4

$$W_{\max} = \sqrt{\frac{4\varepsilon_{\mathrm{SiC}}\varepsilon_0 kT\ln(N_{\mathrm{A}}/n_{\mathrm{i}})}{q^2 N_{\mathrm{A}}}} \tag{2.8}$$

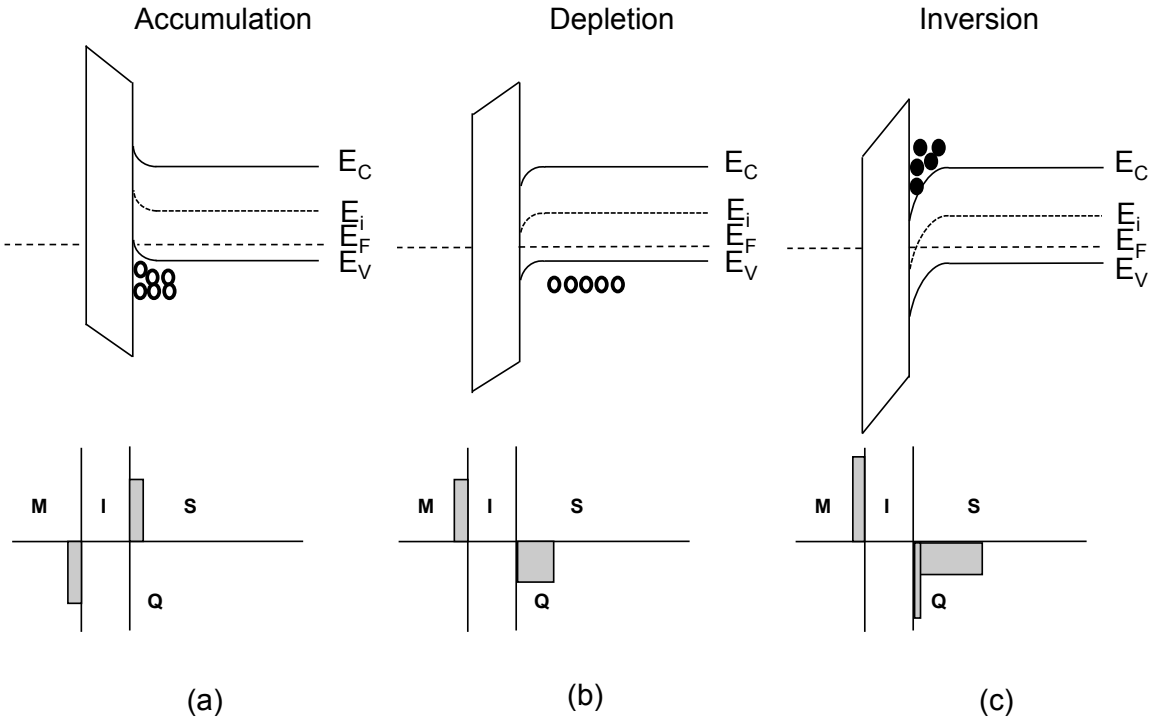


Figure 2.12: Energy band diagrams for p-type MOS structure in different region (a) accumulation, (b) depletion and (c) inversion.

2.5.3 Non-ideal MOS capacitor

In a real MOS system, there are undesirable charges present in the insulator and at the interface, which originate from the imperfection of the surface structure, chemical or impurity related defects and these can affect the electrical properties of the device [114]. In general, there are four types of charge that are of importance in a MOS structure; mobile oxide charge (Q_{m}), fixed oxide charge (Q_{f}), oxide trapped charge and (Q_{ot}), interface trapped charge (Q_{it}) [115]. The basic classifications of traps and charges are shown in Fig 2.13

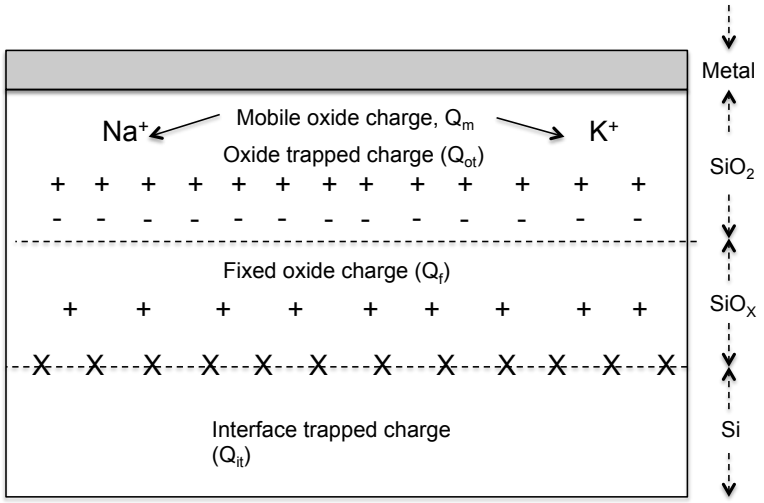


Figure 2.13: Type of charges associated with non-ideal MOS capacitor.

Mobile charge, Q_{m}

Ionic impurities or contaminants such as Na^+, K^+ and Li^+ are the cause for mobile oxide charge. These charges are located in the insulator and can be easily identified using bias stress test.

Fixed oxide charge, Q_{f}

Fixed oxide charges are immobile under applied electric field. They are typically positive and are located near to or at the interface. The origin of these charges is related to the oxidation process. The fixed charge is determined by comparing the difference in the flatband voltage between experimental data and theory. It is not detectable by electrical measurements unless other charges, such as interface trap density and oxide trapped are relatively low.

Oxide trapped charge, Q_{ot}

Oxide trapped charge can be positive or negative. The charges that are trapped in the oxide can be caused by exposure to radiation, Fowler-Nordheim tunnelling or avalanche injection.

Interface trapped charge, Q_{it}

These charges are located at the interface due to structural defects caused by oxidation or other impurities. The charges that are trapped at the interface can be positive or negative. Unlike fixed oxide charge, the density of interface trapped charge varies with gate bias.

2.5.4 Compensation of C-V measurement (series resistance)

The series resistance is formed by the substrate contact on the backside of the wafer and chuck. This resistance significantly affects the results, especially at high frequencies. The series resistance has a negligible impact for substrates that have a very low resistance (less than 10 Ω) but if the backside of the wafer is used as a contact, it can significantly interfere with the results. Consequently, raw data from C-V measurements need to be corrected for series resistance prior to analysis [114]. Series resistance R_s can be calculated from

$$R_{\mathrm{s}} = \frac{(\frac{G_{\mathrm{M}}}{\omega C_{\mathrm{M}}})^2}{\left(1 + (\frac{G_{\mathrm{M}}}{\omega C_{\mathrm{M}}})^2\right) G_{\mathrm{M}}} \tag{2.9}$$

where C_M and G_M are capacitance and conductance maxima and ω is the measurement angular frequency. The compensated capacitance and conductance can be expressed as [116**?**]

$$C_{\mathrm{com}} = \frac{({G_{\mathrm{M}}}^2 + \omega^2 {C_{\mathrm{M}}}^2) C_{\mathrm{M}}}{(\alpha^2 + \omega^2 {C_{\mathrm{M}}}^2} \tag{2.10}$$

$$G_{\mathrm{com}} = \frac{({G_{\mathrm{M}}}^2 + \omega^2 {C_{\mathrm{M}}}^2) \alpha}{(\alpha^2 + \omega^2 {C_{\mathrm{M}}}^2} \tag{2.11}$$

where

$$\alpha = G_{\mathrm{M}} - ({G_{\mathrm{M}}}^2 + \omega^2 {C_{\mathrm{M}}}^2) \tag{2.12}$$

In this thesis, all the device parameters such as V_{FB}, N_{EFF} and D_{it} are extracted after the series resistance correction has been performed.

2.5.5 Extraction of interface state density

When direct current (DC) voltage is applied during C-V measurements from positive to negative, the traps in the depletion and weak inversion regimes change their occupancy depending on the the band bending. For example, considering n-channel MOSFETs fabricated on p-type substrate; in the depletion region, the majority carriers (holes) are close to the Fermi level. In contrast, in the inversion region, as the band bending occurs, the minority carriers are close to the Fermi level and communicate with the traps. The change in trap occupancy with

respect to bias voltage results in an extra capacitance (interface capacitance, $C_{\rm it}$) in comparison to the ideal case. $C_{\rm it}$ can only be measured if the time period of the alternating current (AC) voltage is greater that the trap response time. A number of measurement techniques have been developed to extract interface state density. Therefore, it is important to understand the advantages and disadvantages of the range of techniques in order to choose the right method.

Conductance method

In 1967, Nicollian and Goetzberger proposed the conductance method which gives information on $D_{\rm it}$ in the depletion and weak inversion regimes; the capture cross-section of majority carriers and surface potential fluctuations [97, 117]. This technique measures the equivalent parallel conductance of a MOS capacitor as a function of voltage and frequency as shown in Figure 2.14 (a). The equivalent circuit of MOS capacitor method includes the semiconductor capacitance, $C_{\rm s}$, the interface trap capacitance, $C_{\rm it}$ and the resistance, $R_{\rm it}$ due to the interface traps. This conductance represents the loss mechanism caused by capture and emission of carriers from the interface traps and can be used to extract the interface state density. The circuit in Figure 2.14 (a) can be futher simplified as shown in Figure 2.14 (b), where $C_{\rm p}$ and $G_{\rm p}$ are given by

$$C_{\rm p} = C_{\rm s} + \frac{C_{\rm it}}{1 + (\omega\tau_{\rm it})^2} \tag{2.13}$$

$$\frac{G_{\rm p}}{\omega} = \frac{q\omega\tau_{it}D_{\rm it}}{1 + (\omega\tau_{\rm it})^2} \tag{2.14}$$

The interface trap density can be extracted using approximate expression as

$$\frac{D_{\rm it}}{\omega} = \frac{2.5}{q}\left(\frac{G_{\rm P}}{\omega}\right)_{\rm max} \tag{2.15}$$

This method is also known as the Hill-Coleman technique when used at a single frequency. By assuming the series resistance of the MOS capacitor is negligible, the circuit in Figure 2.14 (b) can be simplified in terms of measured capacitance, $C_{\rm m}$ and measured conductance, $G_{\rm m}$ as

$$\frac{C_{\rm p}}{\omega} = \frac{\omega G_{\rm m} C_{\rm OX}^2}{G_{\rm m}^2 + \omega^2 (C_{\rm OX} - C_{\rm m})^2} \tag{2.16}$$

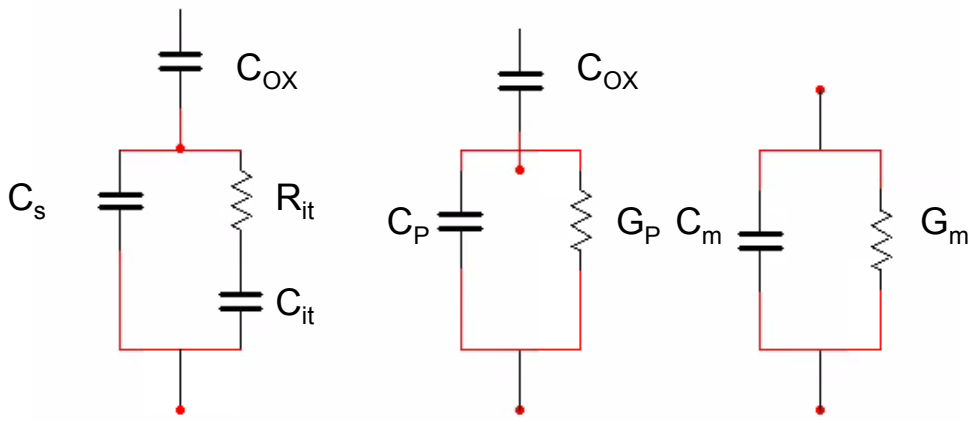


Figure 2.14: Equivalent circuit for conductance measurement; (a) Including interface trap effects, $C_{\rm it}$ and $R_{\rm it}$, (b) simplified circuit of (a), (c) measured circuit.

Terman method

This method compares experimental and theoretical C-V curves. At a very high frequency (typically 1 MHz), the interface traps are assumed not to respond to the excitation used for the C-V measurement but slowly vary with the applied gate voltage. As the interface traps respond to the gate bias, the C-V curves of the high frequency measurement tend to stretch out along the gate voltage axis. This can be described using

$$V_{\rm G} = V_{\rm FB} + \phi_{\rm s} + V_{\rm OX} \tag{2.17}$$

$$\phi_{\rm s} = V_{\rm G} - V_{\rm FB} - V_{\rm OX} \tag{2.18}$$

$$\phi_{\rm s} = V_{\rm G} - V_{\rm FB} - \frac{Q_G}{C_{\rm OX}} \tag{2.19}$$

where,

$$V_{\rm FB} = \phi_{\rm MS} - \frac{Q_{\rm it}}{C_{\rm OX}} \tag{2.20}$$

It is evident that the $\phi_{\rm s}$-$V_{\rm G}$ curve will stretch out when interface traps are present [118]. $D_{\rm it}$ is determined by the difference between the experimental $\phi_{\rm s}$-$V_{\rm G}$ curve and the theoretical $\phi_{\rm s}$-$V_{\rm G}$ curve, as described by

$$D_{\rm it} = \frac{C_{\rm OX}}{q^2}\left(\frac{dV_{\rm G}}{d\phi_{\rm s}} - 1\right) - \frac{C_{\rm s}}{q^2} = \frac{C_{\rm OX}}{q^2}\frac{dV_{\rm G}}{d\phi_{\rm s}} \tag{2.21}$$

However this method has been widely criticized in the determination of D_{it} for SiC because of uncertainties in the capacitance measurement and the use of an insufficiently high frequency for the experimental data. It is also important to know the exact doping density of the semiconductor to calculate the C_{s}.

High-low CV method

In experimental C-V curves, there is a significant frequency dispersion in the depletion regime. The High-Low method extracts D_{it} using the change in C_{it} at different frequencies (high and low) [119], enabling the interface state density to be calculated using

$$D_{\mathrm{it}} = \frac{(C_{\mathrm{D}} + C_{\mathrm{it}})_{\mathrm{LF}} - (C_{\mathrm{D}} + C_{\mathrm{it}})_{\mathrm{HF}}}{Ae^2} \tag{2.22}$$

where $(C_{\mathrm{D}}+ C_{\mathrm{it}})_{\mathrm{LF}}$ is C_{T}–C_{OX} measured at low frequency (1 kHz) and $(C_{\mathrm{D}}+ C_{\mathrm{it}})_{\mathrm{HF}}$ is C_{T}–C_{OX} measured at high frequency (1 MHz). Similar to the Terman method, the high frequency is assumed to have no contribution from interface traps $C_{\mathrm{it}}(\omega_{\mathrm{HF}})\approx 0$ where interface states cannot respond to the high frequency of AC signal as shown in Figure 2.15. This technique must be used with caution for samples with large time constant dispersion [120]. For example, SiC typically has a time constant dispersion two or three times larger than that of silicon. For that reason, this technique is not very suitable for SiC devices.

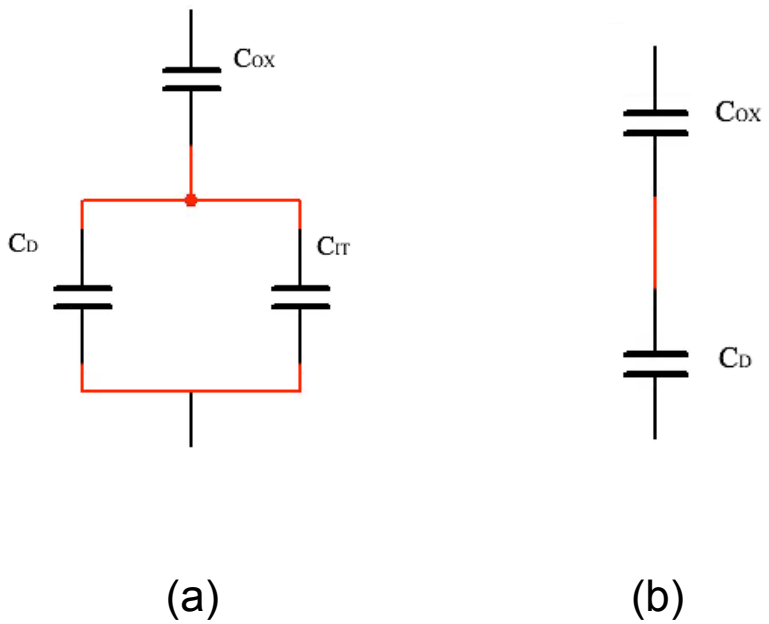


Figure 2.15: Equivalent circuit for low frequency and high frequency.

C-ψ_{s} method

It was reported that the conventional method such as high-low and Terman overestimated the surface potential and this affects the accuracy of the energy level results in underestimation of D_{it}. Furthermore, the fast interface states (generated by NO annealing) that respond at 1MHz cannot be detected by the conventional high$_{(1\mathrm{MHz})}$-low method. Fast interface states can only be detected by increasing the probe frequency, however, a very high frequency measurement is not easily obtained because of parasitics that include series resistance and inductance. Yoshioka introduced a new method called the C-ψ_{s} method to evaluate interface state density in SiC MOS structures using the surface potential based on depletion capacitance [121]. The C-ψ_{s} method is based on the difference between quasi-static (zero frequency) and theoretical capacitances in SiC metal-oxide-semiconductor capacitors and has been shown to accurately determine the interface state density, including the fast states, without the need for high-frequency measurements.

The surface potential (ψ_{s}) can be determined from quasi-static measurement data. The relation between surface potential and gate voltage is given by

$$\psi_{\mathrm{s}}(V_{\mathrm{G}}) = \int \left(1 - \frac{C_{\mathrm{s}}}{C_{\mathrm{OX}}}\right) dV_{\mathrm{G}} + A \tag{2.23}$$

where the integration constant, A, can be determined from the linear extrapolation of $1/(C_{\mathrm{D}}+C_{\mathrm{it}})^2$ versus ψ_{s} using

$$\frac{1}{(C_{\mathrm{D}} + C_{\mathrm{it}})^2} \approx \frac{1}{{C_{\mathrm{dep}}}^2} = \frac{2\psi_{\mathrm{s}}}{A^2 \varepsilon_{\mathrm{SiC}} q N_{\mathrm{D}}} \tag{2.24}$$

The surface potential is used to calculate the theoretical semiconductor capacitance, C_{D},

$$C_{\mathrm{D,theory}}\left(\psi_{\mathrm{s}}\right) = \frac{\mathrm{A}qN_{\mathrm{D}}\left|\exp\left(\frac{q\psi_{\mathrm{s}}}{k_{\mathrm{BT}}}\right) - 1\right|}{\sqrt{\frac{2k_BTN_{\mathrm{D}}}{\varepsilon_{\mathrm{SiC}}}\left\{\exp\left(\frac{q\psi_{\mathrm{s}}}{k_BT}\right) - \left(\frac{q\psi_{\mathrm{s}}}{k_BT}\right) - 1\right\}}} \tag{2.25}$$

The interface state density extracted using C-ψ_{s} is calculated using the difference between the low frequency (quasi static) data where all traps can respond and $C_{D,theory}$ (C_{it}=0) as given below

$$D_{\mathrm{it}} = \frac{(C_{\mathrm{D}} + C_{\mathrm{it}})_{\mathrm{QS}} - (C_{\mathrm{D}} + C_{\mathrm{it}})_{\mathrm{theory}}}{\mathrm{A}e^2} \tag{2.26}$$

Equivalent circuits for the MOS capacitor using the C-ψ_{s} method are shown in Figures 2.16 (a) and (b) respectively.

$(C_{\mathrm{D}}+ C_{\mathrm{it}})_{\mathrm{QS}}$ is C_{D}+C_{it} extracted from quasi static measurements and $(C_{\mathrm{D}})_{\mathrm{theory}}$ is obtained from theoretical calculation of semiconductor capacitance.

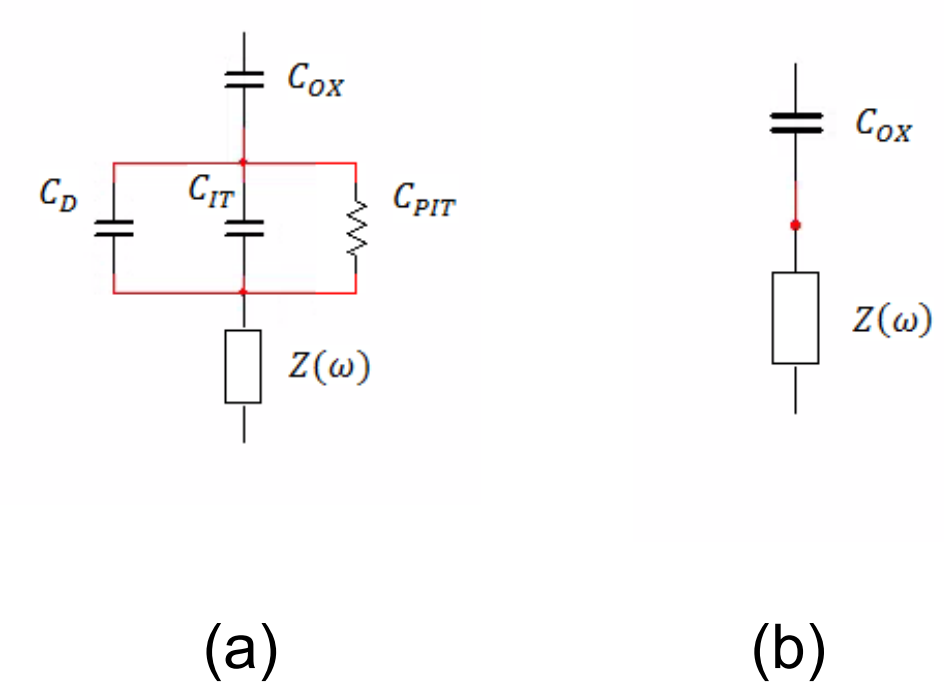


Figure 2.16: Equivalent circuit for a MOS capacitor using C-ψ_{s} method (a) in depletion (b) strong accumulation where C_{D}, C_{OX}, C_{it}, G_{PIT} and Z are the semiconductor capacitance, oxide capacitance, interface-state capacitance, interface-state conductance and parasitic impedance respectively.

2.6 MOSFETs

A MOSFET consists of an MOS capacitor structure with a highly doped source and drain region either side. Figure 2.17 is a schematic of n-channel MOSFET fabricated on a p-type substrate. The MOSFET acts like two p-n junction diodes positioned back-to-back. When $V_{\mathrm{G}} > V_{\mathrm{TH}}$, the semiconductor surface is inverted to n-type, due to the accumulation of minority carriers, which form a conducting channel between the source and drain. Electrons will flow from source to drain when a drain voltage, V_{D} is applied (typically 0.1 V).

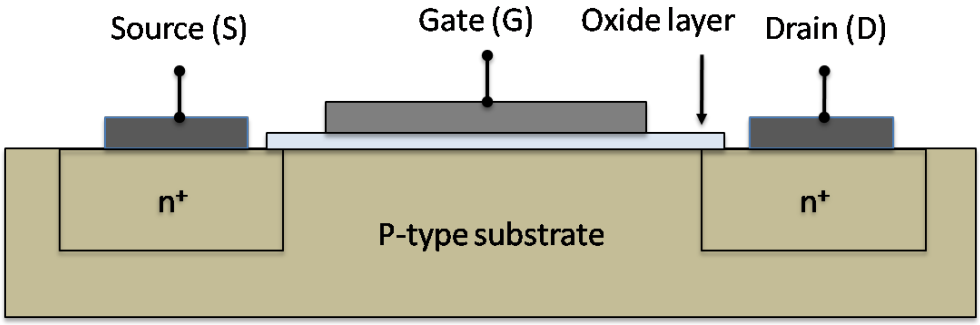


Figure 2.17: Schematic of n-channel MOSFET device structure on p-type substrate

Using the charge sheet approximation, there is no potential drop in a sheet of inversion charge at the semiconductor surface under strong inversion condition. The inversion charge can be written as

$$Q_{\text{inv}} = C_{\text{OX}}(V_{\text{GS}} - V_{\text{TH}} - V_{cs}(x)) \tag{2.27}$$

where $V_{\text{cs}}(x)$ is the channel potential at a position x. The drain current, I_{DS}, flows in the channel is a drift current caused by the lateral electric field, E_{x}. The drain current, I_{DS} can be written as

$$I_{DS} = \frac{Q_{\text{inv}} W L}{t_r} \tag{2.28}$$

where W is the channel width, L the channel length and t_r the carrier transit time.

By assuming the velocity of the carriers is constant, the carrier transit time can be determined

$$t_r = \frac{L}{v} \tag{2.29}$$

It is known that the carrier velocity, v along the channel depends on the lateral electric field, E_{x}, and is related to the carrier mobility by

$$v = \mu\, E_{\text{x}} \tag{2.30}$$

where $E_{\text{x}} = dV_{\text{cs}}(x)/dx$. By combining equations from Equation 2.27 to 2.30, the drain current, I_{DS} can be expressed as

$$I_{DS} = \mu W C_{\mathrm{OX}} dV_c (V_{\mathrm{GS}} - V_{\mathrm{TH}} - V_{cs}(x)) \tag{2.31}$$

By integrating the Eq 2.31 from the source (x=0, V_{cs}(0)=0) to the drain (x=L, $V_{\mathrm{cs}}(L)$=V_{DS}), it is possible to obtain

$$\int_0^L I_{DS} dx = \mu W C_{\mathrm{OX}} \int_0^{V_{\mathrm{DS}}} (V_{\mathrm{GS}} - V_{\mathrm{TH}} - V_{cs}(x)) dV_{cs} \tag{2.32}$$

In the saturation region, where V_{GS}-$V_{\mathrm{TH}} \gg V_{\mathrm{DS}}$, the drain current, I_{DS} can be expressed by

$$I_{DS} = \mu \frac{W}{L} C_{\mathrm{OX}} \left[(V_{\mathrm{GS}} - V_{\mathrm{TH}}) V_{\mathrm{DS}} - \frac{{V_{\mathrm{DS}}}^2}{2} \right] \tag{2.33}$$

Linear region (V_{GS}>V_{TH})

For V_{GS}>V_{TH} and 0<V_{DS}<V_{GS}, the drain current, I_{DS} increases linearly with V_{GS} as the quadratic term, ${V_{\mathrm{DS}}}^2 \approx 0$ can be ignored. The drain current, I_D can be approximated to

$$I_{DS} = \mu \frac{W}{L} C_{\mathrm{OX}} [(V_{\mathrm{GS}} - V_{\mathrm{TH}}) V_{\mathrm{DS}}] \tag{2.34}$$

Saturation region (V_{DS}>V_{GS}-V_{TH})

As V_{DS} is increased, the drain current also increases, but the distribution of the inversion charge becomes nonuniform along the channel. At V_{DS}=V_{GS} - V_T, the Q_{inv} at the drain end become nearly zero resulting in a pinch off (inversion charge per unit area, $\mathrm{Q}_n \approx 0$). As V_{DS} increases further, the pinch-off point will move towards the source, since the potential drop along the channel is also increased. The drain current remains constant once the drain voltage exceeds V_{DS}>V_{GS}-V_T and the MOSFET enters the saturation region where the direction of electric field is the reversal of vertical field applied. The drain current in the saturation region can be written as

$$I_{DS} = \mu \frac{W}{2L} C_{\mathrm{OX}} [(V_{\mathrm{GS}} - V_{\mathrm{TH}})^2] \tag{2.35}$$

2.6.1 Field effect mobility in SiC MOSFETs and scattering mechanisms

The field effect mobility, μ_{EFF} of carriers in a MOSFET channel can be defined as

$$\mu_{\mathrm{EFF}} = \frac{L}{WC_{\mathrm{OX}}V_{\mathrm{DS}}}\left(\frac{dI_{DS}}{dV_{GS}}\right) \tag{2.36}$$

where I_{DS}, V_{DS} and are the drain current, drain voltage and gate voltage respectively. The MOSFET transconductance is defined as

$$g_m = \frac{dI_{DS}}{dV_{GS}} \tag{2.37}$$

Since the interface state density in a SiC MOS structure is high (10^{13} cm^{-2}eV^{-1}), typically of the same order as the sheet electron density, 10^{12} cm^{-2}. Once the traps are fully occupied, less than 10% of the electron can travel from the source to drain and this results in a low field effect mobility of approximately 10 cm^2/V.s. The mobility is limited by several scattering mechanisms including Coulomb scattering, phonon scattering, surface roughness scattering and bulk mobility scattering that are pertinent to MOSFETs operating at different electric fieldsS and temperatures. The sum of each reciprocal mobility component is proportional to the reciprocal of total mobility as given by Matthiessen's rule [122, 123],

$$\frac{1}{\mu_{\mathrm{T}}} = \frac{1}{\mu_{\mathrm{C}}} + \frac{1}{\mu_{\mathrm{SR}}} + \frac{1}{\mu_{\mathrm{SP}}} + \frac{1}{\mu_{\mathrm{B}}} \tag{2.38}$$

where μ_{C} is Coulomb mobility, μ_{SR} is surface roughness mobility, μ_{SP} is phonon mobility and μ_{B} is bulk mobility. For 4H-SiC MOSFET, the bulk mobility scattering has a negligible influence on the field effect mobility, because other scattering mechanisms are dominant at the oxide/semiconductor interface. Figure 2.18 shows the contribution of the 3 dominant scattering mechanisms that limit the field effect mobility. Under low electric fields, Coulomb scattering from the fixed and trapped charge at the SiC/SiO_2 interface is the most prominent. Surface phonon scattering is the deflection of electrons by acoustic phonon at the semiconductor surface. However, this is it not the limiting factor for field effect mobility in 4H-SiC MOSFETs. The existence of step bunching on the surface of off angle 4H-SiC wafers makes the interface SiC/SiO_2 very complex and rough which results in a significant degradation of the field effect mobility under high electric fields, limited by surface roughness scattering. Electrons flowing in the channel (near or at the SiC/SiO_2 interface) experience more surface roughness scattering at high electric fields (perpendicular to the surface) because electrons are strongly attracted to the SiC surface or interface as the electric field increases. Therefore, the field effect mobility is determined by the interplay of several mechanisms that are typically affected by device processing.

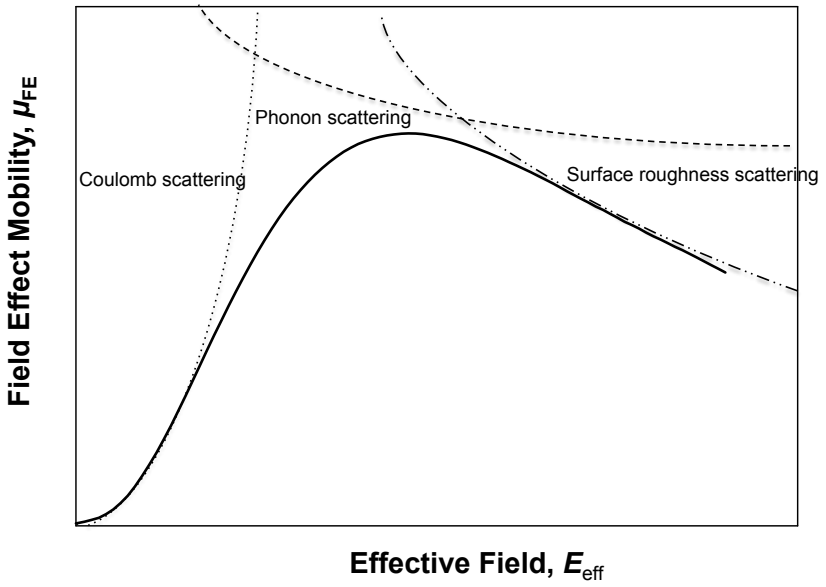


Figure 2.18: Scattering mechanisms that are affecting the field effect mobility in MOSFET.

2.6.2 Correlation between subthreshold slope and interface state density

Subthreshold swing, (S) is a parameter to quantify how sharply the transistor is turn on or off. It can be calculated as

$$S = (\ln 10)\frac{dV_{\mathrm{G}}}{d(\ln I_{\mathrm{D}})} \tag{2.39}$$

$$S = \ln(10)\frac{kT}{q}\left(1 + \frac{C_{\mathrm{D}}}{C_{\mathrm{OX}}}\right) \tag{2.40}$$

where $\mathrm{C_D}$ is depletion layer capacitance and C_{OX} the oxide capacitance. In the case of zero oxide thickness, the characteristic is identical to the case of diffusion current in a p-n junction. For nonzero oxide thickness, the swing is degraded by a voltage divider of two capacitors in series, whose ratio is (C_{OX} + C_{D}) / C_{OX}. In the presence of D_{it}, the C_{it} is in parallel with the depletion capacitance, C_{D}. By substituting C_{OX} + C_{D} for C_{D}, the S can be shown as

$$\begin{aligned} S(\text{with } D_{\mathrm{it}}) &= \ln(10)\frac{kT}{q}\left(\frac{C_{\mathrm{D}} + C_{\mathrm{OX}} + C_{\mathrm{it}}}{C_{\mathrm{OX}}}\right) \\ &= S(\text{without } D_{\mathrm{it}}) \times \frac{C_{\mathrm{D}} + C_{\mathrm{OX}} + C_{\mathrm{it}}}{C_{\mathrm{OX}}} \end{aligned} \tag{2.41}$$

It is necessary to have low doping, thin oxide and low interface trap density for a sharp subthreshold slope or small S. The data in Fig 2.19 show the influence of $D_{\rm it}$ to the subthreshold slope or transfer characteristics of samples with and without $D_{\rm it}$.

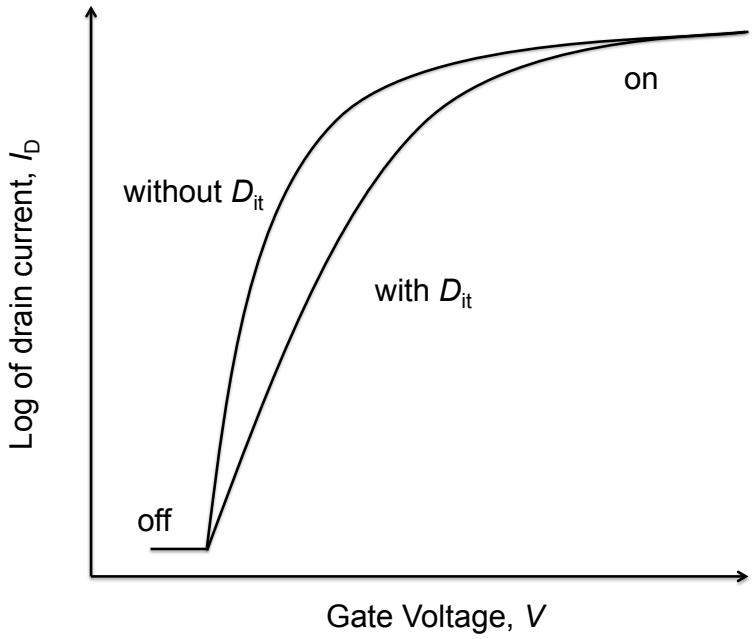


Figure 2.19: Transfer characteristic ($I_{\rm D}$-$V_{\rm G}$) with and without $D_{\rm it}$.

From a plot of log $I_{\rm D}$-$V_{\rm G}$, $D_{\rm it}$ can be obtained requring an accurate value of $C_{\rm OX}$ and $C_{\rm b}$ as

$$D_{\rm it} = \frac{C_{\rm OX}}{q^2}\left(\frac{qS}{\ln(10)kT} - 1\right) - \frac{C_{\rm b}}{q^2} \tag{2.42}$$

2.6.3 Interface properties of the oxide / SiC interface on different crystallographics faces

4H-SiC has more than one crystal face. Many attempts have been made to reduce $D_{\rm it}$ and improve channel mobility on the (0001) Si-face of 4H-SiC. Nevertheless, the channel mobility is still significantly lower than the bulk carrier mobility. It has been reported that utilization of other planes of 4H-SiC including $(000\bar{1})$, $(11\bar{2}0)$ and $(1\bar{1}00)$ result in higher channel mobility due to the differences in the distribution of the interface states density near the conduction band [50]. The data in Figure 2.20 show the field effect mobility as a function of the oxide field on n-channel MOSFETs, fabricated on 4H-SiC using the same fabrication process. The obtained field effect mobilities on the other faces, $(000\bar{1})$ with 45 cm^2/V.s and $(11\bar{2}0)$ with 100 cm^2/V.s, are significantly higher than those obtained on (0001) with 25 cm^2/V.s. The

result from the $(11\bar{2}0)$ face is very promising for the development of trench MOSFETs on SiC (0001) wafers.

The use of sidewall planes is an attractive way to increase the channel mobility of 4H-SiC MOSFETs due to the low interface state density near the conduction band [124]. The sidewall plane of (0001) such as $(11\bar{2}0)$ has been used to develop trench structures for the application of power MOSFETs [125, 126]. However, to date there are limited reports concerning the potential of sidewall planes integrated with top planar surface to realise the enhancement of drain current on the same footprint area; 3-D gate structure MOSFETs [127].

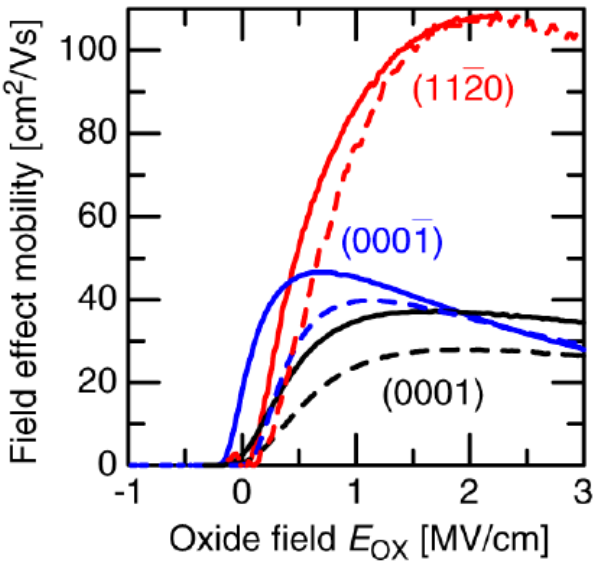


Figure 2.20: Field effect mobility as a function of oxide field on n-channel MOSFETs fabricated on 4H-SiC with different face orientation of (0001), $(000\bar{1})$ and $(11\bar{2}0)$. Graph was taken from [50].

2.7 Multi-gate transistor/ FinFET

According to Moore's law, the number of transistors on a given area doubles every two years [128]. As sub nanometer length scales are approached, due to short channel effects (SCE), off-state leakage (current that leaks through transistors even when they are turned off) has become a big issue [128, 129]. There are two principal components of static power consumption; subthreshold leakage current and gate leakage [130]. Suppressing the leakage current during the off-state is important for the management of power consumption. Multi-gate transistors or FinFETs have been shown to effectively provide a greater level control of the

channel and hence reduce the leakage current through the body in the off-state [131]. In silicon technology, the FinFET was originally introduced to evade the short channel effects (SCE) such as hot electron effects, drain induced barrier lowering (DIBL) and surface scattering. As shown in Figure 2.21, the FinFET is a new generation transistor that employs a 3-gate structure [132, 133]. It has an advantage in the effective width of the channel where the transistor height can increase the current capability, however it is very challenging to significantly increase the height of the fins, since there many physical and fabrication issues.

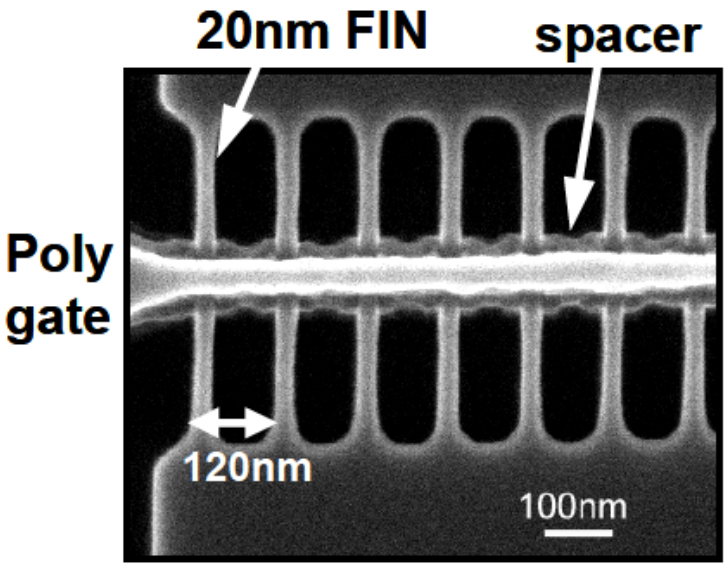


Figure 2.21: SEM image of FinFET with multi fins at a 120 nm pitch using e-beam lithography. Image was taken from [134].

The multigate MOSFET is one of the encouraging solutions that meets International Technology Roadmap for Semiconductors (ITRS) roadmap requirements for the reduction of short channel effect in silicon MOSFETs [135]. A diversity of new architectures of multi gate devices has been proposed recently including Double Gate, Gate All Around, Omega FET, Pi FET and FinFET [136]. The effect of drain potential on the channel can be reduced effectively, as a result of the superior control from the additional gates. Due to the large effective channel width, the drain current of multi gate SiC MOSFETs is higher than a conventional planar MOSFET. The current will be further enhanced by the higher field effect mobility on the sidewall planes of 4H-SiC, $(11\bar{2}0)$ and $(1\bar{1}000)$ [127, 137]. Due to the ability of supressing the short channel effects and relatively simple fabrication steps, SiC FinFET has attracted huge attention in the field of wide bandgap semiconductor devices [138].

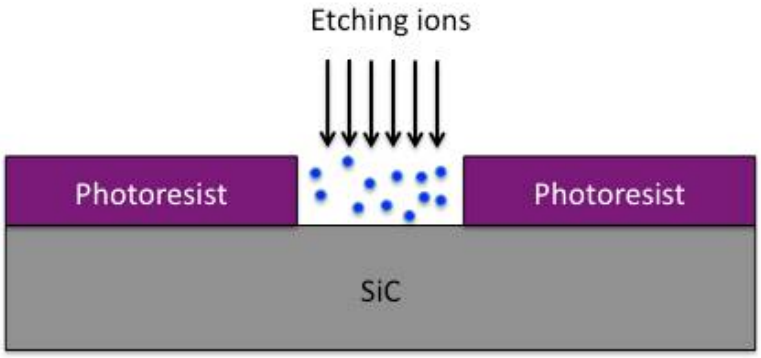


Figure 2.22: Reactive ion etching (RIE) using photoresist as a mask.

2.7.1 Etching

Fabrication of narrow fin / 3-D structures with smooth sidewalls is one of the primary challenges in SiC due to its chemical inertness. Therefore, it is very difficult to etch SiC using wet chemistry. There are some techniques can be used to etch SiC such as electrochemical process, employing molten fluxes, hot gases and plasma etching, however these are not practical for the realisation of repeatable submicron features.

Inductively coupled plasma (ICP) and electron cyclotron resonance (ECR) have been reported to have a higher rate of etch in comparison to reactive ion etching (RIE) [139]. RIE is one type of plasma etching that has been utilized to break the bonds in the material. A lot of materials can be etched using this method including SiO_2, silicon based materials, metals and diamond. To avoid re-deposition of foreign material onto the substrates a quartz or graphite cover plate is usually used and gas is injected into the chamber via a shower head gas inlet. RIE is suitable for patterning small features ($\ll 1$ μm) because it is an anisotropic etching [13]. The R.F. source (bottom electrode) attracts the electrons, charging it negatively and this produces ion clouds that will accelerate toward the sample. Different to the plasma etching where ions move randomly in the chamber, in RIE ions move in the direction controlled by electric field that make anisotropic etching to happen (see Fig 2.22).

2.8 Summary

The history and material properties of SiC have been reviewed, encompassing the key issue and challenges with the technology. One of the challenges that limit the development of SiC technology is the cost. It is important for the material quality to improve as well as

the wafer size to bring further increase in device yield which will result in lower cost. It is also essential to address the issue of the high density of interface traps at the SiC/SiO_2 interface that is known to lower the channel mobility of SiC MOSFETs. Post oxide annealing (POA) is a technique to reduce the interface trap density by passivating the unsatisfied bonds at the SiC/SiO_2 interface. High-κ materials including Al_2O_3, TiO_2 and HfO_2 are an interesting alternative to increase the channel mobility with ALD offering excellent uniformity on any type of substrates. Experimental results have shown that the different facets of SiC including $(1\bar{1}00)$ and $(11\bar{2}0)$ face exhibit high channel mobility. Multigate FinFET structures provide a greater device width per unit area and ensure excellent electrostatic integrity. Despite having a primary challenge in the device fabrication, it is really a promising direction for achieving higher current. Finally, utilizing currently advanced characterization and analysis techniques, further information can be obtained to produce better SiC devices.

Chapter 3

Phosphorus doped SiO_2 / 4H-SiC MOS capacitors

Part of the results in the chapter were published in the Journal of Applied Physics, **120**, 214902 (2016)

3.1 Introduction: Instability of phosphorus doped SiO_2 in 4H-SiC MOS capacitors at high temperatures

In the history of high temperature electronics, silicon technology has been used with a limited operating capability of temperatures below 150°C [19]. The demand for electronic components that are capable of sustaining high temperature operation for markets such as automotive, aerospace, energy generation and military has been growing rapidly. Due to the excellent material properties of SiC, such as the extremely low intrinsic carrier density (intrinsic carrier concentration increases exponentially with temperature. A material that has low intrinsic carrier concentration still can keep the n_i lower than extrinsic doping concentration. Due to that reason SiC electronic devices can operate at high temperature with low leakage current), the feasibility to grow a thermal oxide and wide bandgap; it has become a leading candidate for high temperature and high power electronics. A lot of effort to improve the quality, performance and reliability of silicon carbide MOS structures has been made, especially focusing on the quality of the gate oxide, which plays a vital role in the performance of SiC MOSFETs. However, in recent years a number of issues have been reported with SiC MOSFETs, especially in terms of performance and long term reliability [30, 140]. These issues have been gradually alleviated as a result of recent developments. One of the significant remaining issues with silicon carbide MOSFETs is the low channel mobility caused by Coulomb scattering and trapping that increases the subthreshold swing, S and threshold voltage, V_{TH} [67, 141]. Many researchers have been working on increasing the channel mobility of SiC MOSFET by optimizing passivation techniques using nitrogen [50, 58], sodium [81] and phosphorus [2, 4] rich environments. It has been shown [58, 142] that the inversion channel mobility within SiC dramatically improves when the $(11\bar{2}0)$ face is utilised due to surface morphology (no step bunching) [124] and charge distribution, although this leads to a decrease in threshold voltage which for some applications may be undesirable.

Threshold instability is one of the important factors that disrupts the performance and reliability of SiC MOSFET. Recently, the threshold voltage instability for MOSFET annealed in $POCl_3$ has been investigated by using both positive and negative bias at temperatures up to 200°C [42]. The data were described by a model based on the capture and emission properties of traps at the SiO_2/SiC interface or in the bulk oxide. It has been confirmed that the main origin of the threshold voltage instability is the oxide traps in phosphorus-doped oxides.

It has been reported that incorporating P atoms into the SiO_2/SiC interface reduces the D_{it} near the conduction band and increases the field effect mobility to 89 cm^2/V.s [2]. Linked to this experimental result, a reduction in the interface state density was observed for samples (n-channel devices) implanted with P prior to oxidation [2]. It is reported that the incorporated P atoms reduce the strain and lead to a reduction of the trap density at the SiO_2/SiC interface [2, 38]. Liu also reported that passivation of the SiO_2/SiC interface using phosphorus results in lower D_{it} and higher field effect mobility than nitrogen passivation for MOSFETs fabricated on both the Si face and the $(11\bar{2}0)$ a-face of 4H-SiC [58]. However, the mechanism responsible for D_{it} reduction by P incorporation is still not fully understood.

Atoms in group 5 of the periodic table consist of nitrogen (N), phosphorus (P), arsenic (As), antimony (Sb), and bismuth (Bi) and each has 5 electrons in the outermost shell. This electron configuration provides 4 half-filled outer orbitals that can interact with lone pairs of other elements to form 4 covalent bonds. According to Density Functional Theory (DFT) calculations, strong silicon-nitrogen, silicon-phosphorus and silicon-arsenic bonds are created at the SiC/SiO_2 interface, resulting in a decrease in the density of near interface traps [143]. Observations from X-ray photoelectron spectroscopy (XPS) and electrically detected magnetic resonance (EDMR) spectroscopy also imply that N and P atoms can not only passivate interfacial defects, but may also diffuse into the SiC substrate resulting in an increased channel mobility and reduction in threshold voltage, through the creation of shallow donors (the energy level is not provided by the literature) [58, 144, 145]. The occurrence of counter-doping of the SiC surface has been proposed, where a very thin n-type layer is formed at the SiC/SiO_2 interface due to the incorporation of N or P atoms [58].

The conductivity of the SiC surface after being exposed to post-oxidation annealing (POA) in N_2O and $POCl_3$ has been examined qualitatively by using scanning spreading resistance microscopy (SSRM) measurements [146]. It was found that the incorporation of P-related shallow donors after POA in $POCl_3$ is greater than N-shallow donors incorporation during N_2O treatment, which subsequently explains the significantly enhanced channel conductivity

of the MOSFETs. The quantitative analysis of the doping at the SiO_2/SiC interface to explain the functional doping effect from N and P atoms was performed using electrostatic simulations [147]. The counter-doping effect was assumed to arise from a thin layer of n-type material in the p-well region. By varying the thickness and doping concentration, it was identified that the counter-doping reduces the electric field at the interface, alleviating the effect of surface roughness, resulting in higher mobility, but resulted in instability in threshold voltage (V_{TH}), flatband voltage (V_{FB}) and effective oxide charge (N_{EFF}).

Because of the suitability of SiC for the realisation of high temperature electronic devices, the reliability and high temperature performance of phosphorus incorporated SiO_2 in 4H-SiC is of increasing interest. However to date very little attention has been paid to the performance of phosphorus doped oxides at high temperatures. The data in this thesis reports on the flatband, threshold voltage and oxide charge shift (hysteresis) for phosphorus incorporated MOS (by characterizing bidirectional C-V curves at different frequencies between 10 kHz and 1MHz) at temperatures up to 300°C. All the extracted parameters were compared to an undoped thermal oxide gate dielectric sample to determine the effect of phosphorus incorporation on the oxide characteristics.

3.1.1 Experimental and evaluation method

In this work two Si-face, 4° off axis, 4H-SiC wafers 4 μm epilayer thickness with N_{D} = 1.44 $\times$ 10^{17} cm^{-3} (provided by Raytheon) with different gate dielectric fabrication process were compared. sample 1 was prepared with a thermal gate oxide that has been through a conventional post-oxide annealing process [148]. sample 2 is a phosphorus doped gate oxide structure which was annealed using a planar source of phosphorus pentoxide (P_2O_5) after thermal oxidation. Both wafer processes are designed to be compatible with a commercial CMOS process [149]. Process details and the equivalent oxide thickness of the SiO_2 for both wafers are summarized in Table 3.1.

A Keithley 4200 SCS was used to measure capacitance-voltage (C-V) at different frequencies and elevated temperatures. The measurement was swept from accumulation (+10 V) to depletion (−10 V) (reverse sweep) and vice versa (forward sweep) under positive and negative bias conditions. In this experiment, the flatband voltage (V_{FB}) was determined by calculating the flatband capacitance, C_{B} using

Table 3.1: Summary of fabrication process for both samples.

Wafer	Metal	Gate dielectric	Effective T_{OX} (nm)	Size (μm^2)
1	Aluminium	Thermal oxide + anneal + nitride cap	33.0	1.12×10^5
2	Aluminium	Thermal oxide + anneal (PHOS source) + nitride cap	35.7	1.12×10^5

$$C_{\mathrm{B}} = \frac{C_{\mathrm{OX}}\varepsilon_s A/L_{\mathrm{D}}}{C_{\mathrm{OX}} + \varepsilon_s A/L_{\mathrm{D}}}, \tag{3.1}$$

where ε_s is the permittivity of the silicon carbide (taken as equal to 9.7 ε_0 [55]), C_{OX} the experimental oxide capacitance and L_{D} is the Debye length which can be expressed as:

$$L_{\mathrm{D}} = \sqrt{\frac{k_{\mathrm{B}}T\varepsilon_s}{q^2 N_{\mathrm{D}}}}, \tag{3.2}$$

where k_B is the Boltzmann constant, T is the absolute temperature and N_{D} is the doping concentration. The flatband voltage is extracted directly from the capacitance-voltage characteristic.

A significant effort has been focussed on trying to improve the quality of the SiC/SiO_2 interface by reducing the total effective oxide charge and the interface state density, because these two parameters determine the carrier channel mobility and gate leakage current. During MOSFET operation, the density and position of charged centres in the gate oxide change, resulting in the observed stability and reliability problems. Effective oxide charge, Q_{EFF}, is used to describe the charge trapped in the bulk of the dielectric and is computed from the sum of the fixed oxide charge (Q_F), mobile ionic charge (Q_M) and oxide-trapped charge (Q_{OT}). Q_{EFF} does not vary with gate voltage, unlike interface trapped charge (Q_{IT}) and it can be assumed that the charges exist in the bulk of the SiO_2.

$$Q_{\mathrm{EFF}} = Q_{\mathrm{F}} + Q_{\mathrm{M}} + Q_{\mathrm{OT}} \tag{3.3}$$

In order to extract Q_{EFF}, high-frequency room temperature capacitance–voltage characterization was performed at 1 MHz. The effective oxide charge was obtained using

$$Q_{\mathrm{EFF}} = C_{\mathrm{OX}}(W_{\mathrm{MS}} - V_{\mathrm{FB}}), \tag{3.4}$$

Where W_{MS} is the metal-semiconductor work function with a value in eV, (the work function used for Al is 4.1 eV and the electron affinity of SiC is 3.1 eV (Ref.[150]), C_{OX} is the experimental oxide capacitance per unit area and V_{FB} is the flatband voltage. The effective oxide charge density, N_{EFF} can be calculated as

$$N_{\mathrm{EFF}} = \frac{Q_{\mathrm{EFF}}}{q}. \tag{3.5}$$

where q is electron charge (1.602 $\times$ 10^{-19} C). In SiC MOS capacitors, the inversion capacitance cannot be measured due to the low intrinsic carrier concentration and hence low generation rate of minority carriers [11, 28]. The turn-on region of a MOSFET correlates to the inversion region in C-V measurement data. The threshold voltage, V_{TH} can be determined from the flatband voltage by Eq. 3.6

$$V_{TH} = V_{\mathrm{FB}} \pm \left[\frac{A}{C_{\mathrm{OX}}} \sqrt{4\varepsilon_s q |N_{\mathrm{D}} \Phi_{\mathrm{B}}|} + 2|\Phi_{\mathrm{B}}| \right], \tag{3.6}$$

where A is the gate area, N_{D} is doping concentration and V_{FB} is the flatband potential. Φ_{B} is the bulk potential calculated from

$$\Phi_{\mathrm{B}} = \frac{k_{\mathrm{B}}T}{q} \ln \left(\frac{N_{\mathrm{D}}}{n_{\mathrm{i}}} \right) \tag{3.7}$$

where n_i is the intrinsic carrier concentration. However, the calculated threshold voltage V_{TH} may be slightly different to threshold voltage V_{TH} for a MOSFET owing to the variety in methods used to extract the threshold voltage.

3.1.2 Results and discussion

Capacitance voltage characterization (room temperature)

The data in Fig. 3.1 show the room temperature C-V characteristics of MOS capacitors fabricated on both wafers. The quasi–static capacitance was measured with a hold time of 10 s. The gate voltage was swept from depletion (-10 V) to accumulation (10 V) at a rate of about 0.1 V/s for the voltage–sweep measurements. In each figure, the quasi–static and

high frequency (1 MHz) C-V data are plotted with a theoretical curve, which was calculated using [114, 151],

$$C_{\mathrm{D,theory}}\left(\psi_s\right) = \frac{AqN_{\mathrm{D}}\left|\exp\left(\frac{q\psi_s}{k_{\mathrm{BT}}}\right)-1\right|}{\sqrt{\frac{2k_BTN_{\mathrm{D}}}{\varepsilon_{SiC}}\left\{\exp\left(\frac{q\psi_s}{k_{\mathrm{B}}T}\right)-\left(\frac{q\psi_s}{k_{\mathrm{B}}T}\right)-1\right\}}} \tag{3.8}$$

The effective oxide charge concentrations, N_{EFF}, were calculated to be -3.26×10^{11} cm^{-2} for the undoped oxide and -3.03×10^{11}cm^{-2} for the phosphorus doped oxide. At room temperature, both samples have negative values of the order of $\sim3\times10^{11}$ cm^{-2}. Phosphorus may reduce the effective oxide charge by passivating dangling bonds at the interface, however the difference is minor in this case. Since the effective oxide charge is the sum of fixed, mobile and trapped charge, [32, 150] further analysis is required to identify the relative contributions from the constituent components. Herein, the temperature dependence of the effective oxide charge, flatband and threshold voltage were studied to determine the effect of phosphorus incorporation on the characteristics of the SiO_2/SiC interface.

Capacitance voltage characterization (elevated temperatures)

In order to investigate the polarization of the gate dielectric and temperature dependence of phosphorus incorporated oxide parameters, 1 MHz capacitance voltage characteristics were measured at temperatures up to 300°C. As can be observed from the data in Fig. 3.2, the C-V data show a shift in flatband voltage for both samples with temperature. The data indicate that the shift in V_{FB} is larger for the phosphorus doped dielectric, indicating a shift in effective oxide charge and the existence of electron trapping, either at the SiO_2/SiC interface or in the bulk oxide. The effect of phosphorus incorporation on the characteristics was investigated by extracting the shift in V_{FB}, V_{TH} and N_{EFF} arising from positive gate bias bidirectional depletion to accumulation (forward sweep) and accumulation to depletion (reverse sweep) voltage sweeps and negative gate bias bidirectional accumulation to depletion (reverse sweep) and depletion to accumulation (forward sweep) voltage sweeps. ΔV_{FB}, ΔV_{TH} and ΔN_{EFF} are defined as the difference in values from those obtained at room temperature; the forward sweep data of V_{FB}, V_{TH}, and N_{EFF} at room temperature are always compared to the forward sweep of V_{FB}, V_{TH}, and N_{EFF} at elevated temperature and vice versa. All the measurements were performed on fresh samples, meaning that the capacitors had not undergone any previous electrical stressing and measurements.

Capacitance voltage hysteresis at room and 300°C

The data in Fig 3.3 show the bidirectional C-V curves for both samples at room and 300°C.

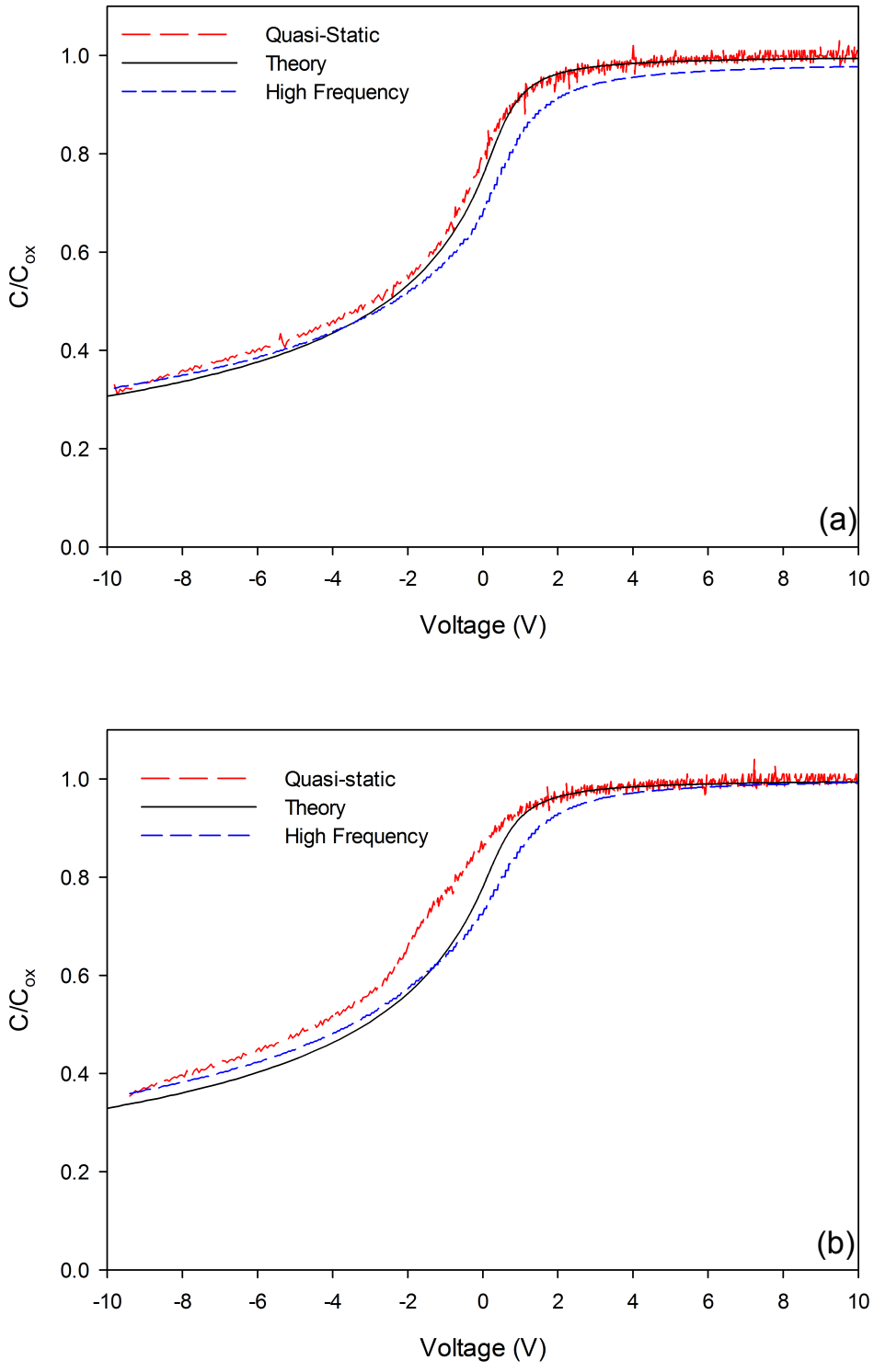


Figure 3.1: Room temperature C-V characteristics of 4H-SiC MOS capacitors (a) undoped gate dielectric (b) phosphorus doped gate dielectric. Experimental quasi–static and high frequency (1MHz) data are plotted with a theoretical curve.

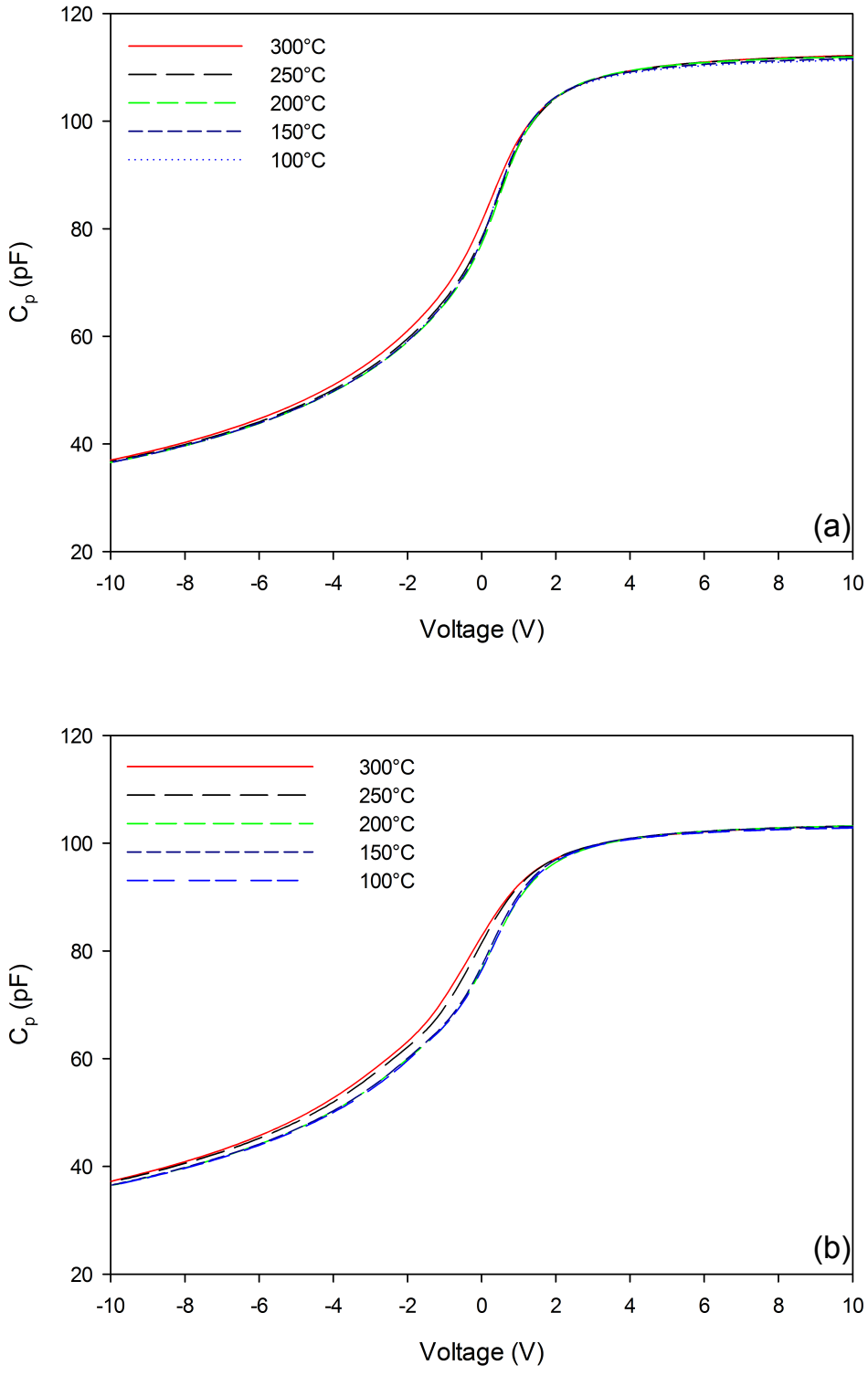


Figure 3.2: 1MHz Capacitance Voltage characteristics of undoped (a) and phosphorus doped devices (b) measured at temperatures between 100°C and 300°C.

Hysteresis is negligible for both samples at the room temperature but it is increasing with the increasing temperature (only the data for 300°C are shown here). At room temperature,

both samples show clock-wise hysteresis originating from the slow trapping (slow states) near SiO_2/SiC interface [54]. The hysteresis is negligible for sample 1 and approximately 0.5 V for sample 2. As the temperature is increased, the direction of C-V hysteresis for both samples remains same with sample 1 shows marginal hysteresis approximately 0.4 V in comparison to sample 2 with approximately 2.2 V. The density of the slow oxide trap, $N_{\rm ot}$ can extracted as

$$N_{\rm ot} = \frac{\Delta V_{\rm FB} \times C_{\rm OX}}{q} \tag{3.9}$$

where $\Delta V_{\rm FB}$ is the shift between the forward and backward C-V curves. The $N_{\rm ot}$ for samples 1 and 2 at 300°C are approximately 2×10^{10} and 1×10^{11} respectively.

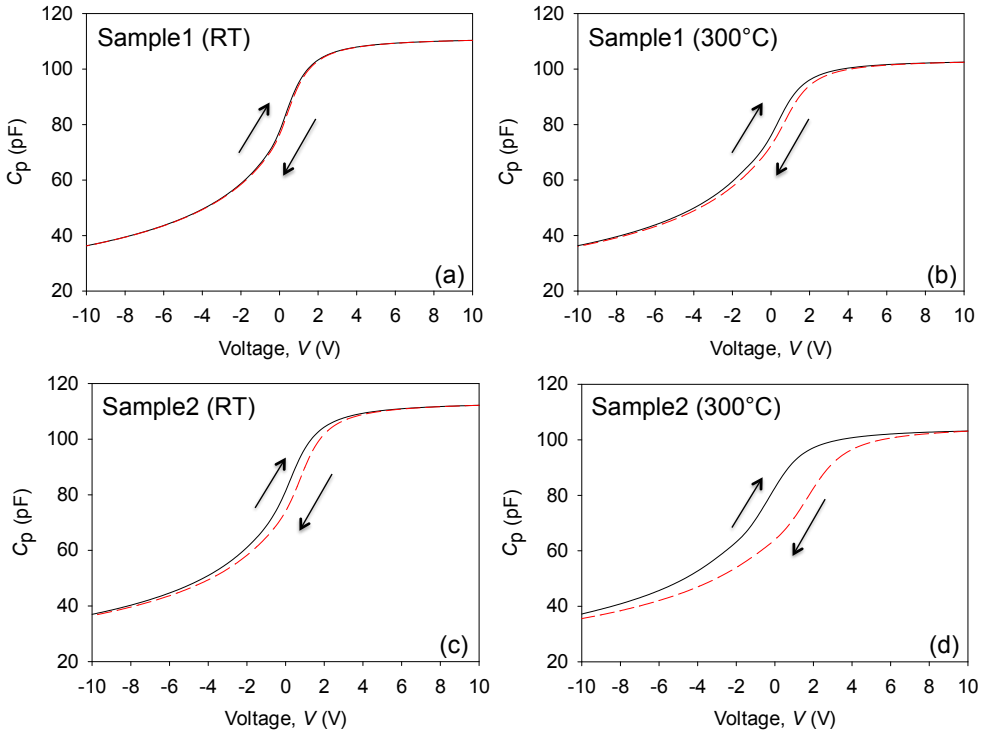
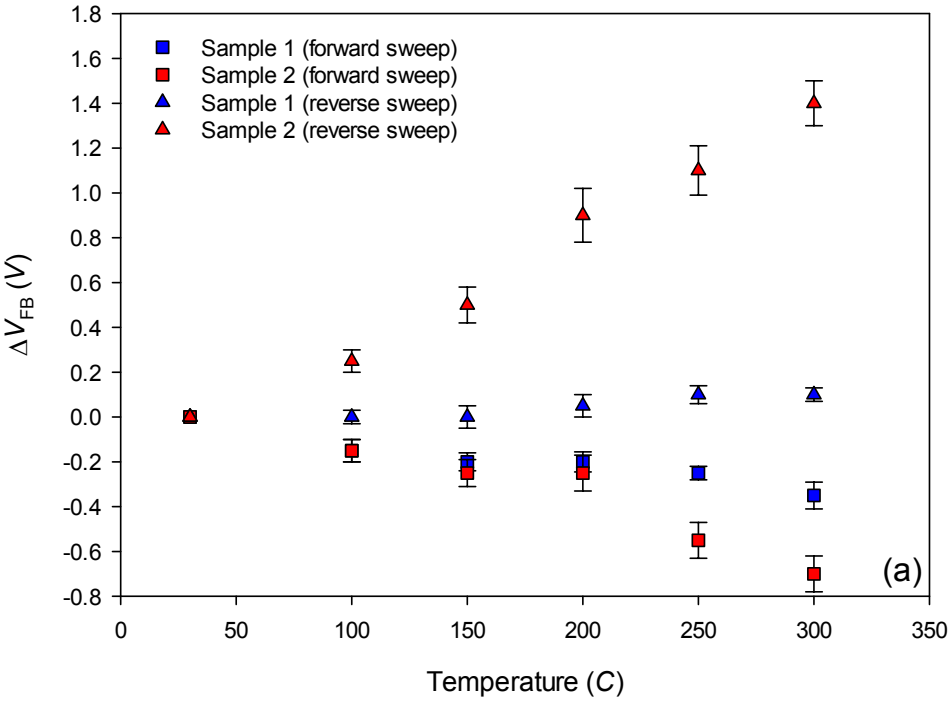


Figure 3.3: 1MHz bidirectional Capacitance Voltage characteristics (hysteresis) of (a) undoped devices at room temperature (b) undoped devices at 300°C (c) phosphorus doped devices at room temperature (d) phosphorus doped devices at 300°C.

3.1.3 Flatband voltage, $V_{\rm FB}$ instability

The data presented in Fig. 3.4 show the change in the extracted flatband voltage highlighting the differences arising from the direction of the voltage sweep. The data in the Fig. 3.4



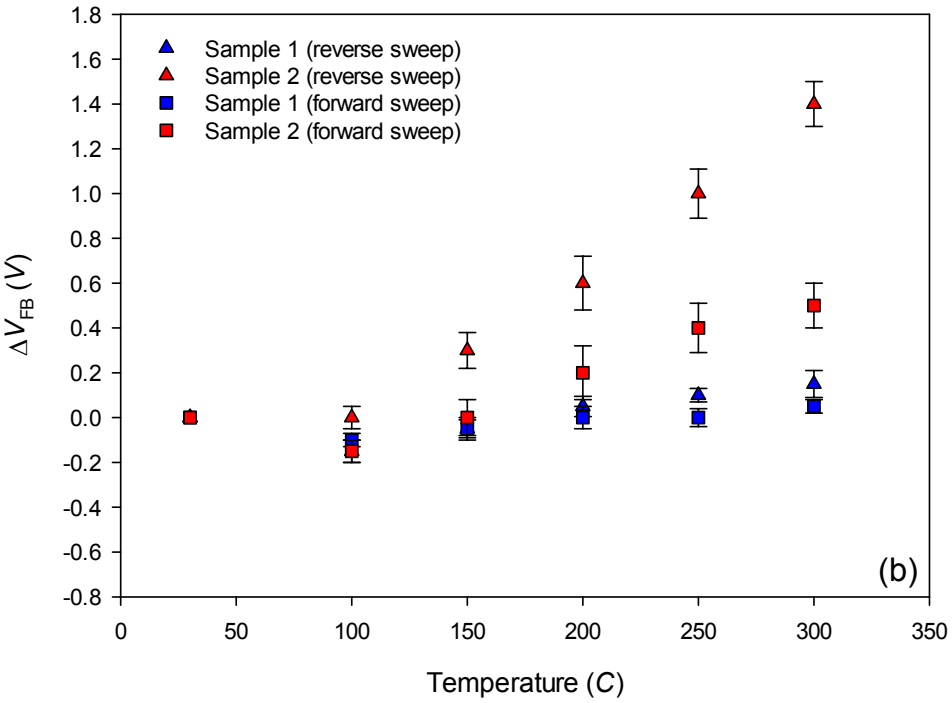
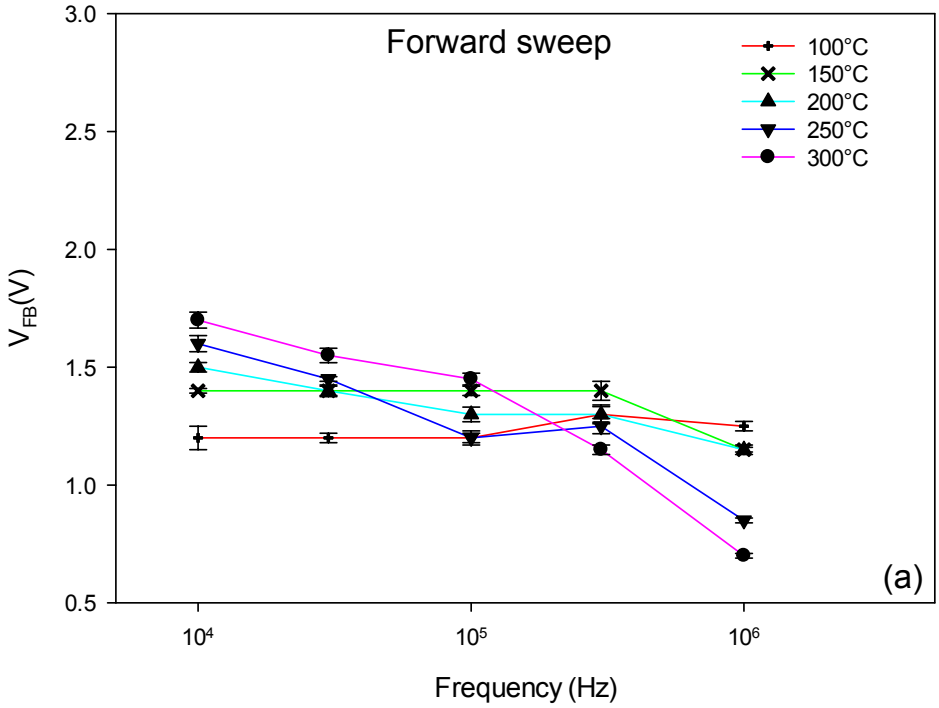


Figure 3.4: Change in flatband voltage ΔV_{FB} extracted from 1 MHz C-V characteristics as a function of temperature for undoped and phosphorus doped dielectrics under (a) negative and (b) positive gate bias conditions. ΔV_{FB} is defined as the difference of V_{FB} at room temperature and those V_{FB} obtained at elevated temperature.

show that the difference in flatband voltage for the phosphorus doped dielectric is more than a factor of four greater than that observed in the undoped dielectric (for both gate bias), which has only a small shift at all temperatures between room temperature and 300°C. The shift is particularly significant for the reverse sweep during the C-V measurements. Positive V_{FB} shifts in the reverse sweep data (red triangles) were also observed, in close agreement with previously reported data for PSG oxides on Si where the observed shift in the C-V characteristics are significant. This is possibly due to the polarization of the PSG doped oxide layer that alters the surface potential of the semiconductor and results in a flatband voltage shift [3] . However, from the results of flatband voltage shift from negative and positive bias measurements (accumulation to depletion and backward and depletion to accumulation and backward), where the flatband shift of sample 2 are to the positive direction regardless of the applied bias stress (bias independent), it is concluded that the instability of phosphorus-doped SiO_2 is due to charge trapping or mobile charge rather than polarization effect where a bias dependent shift is expected. When V_g was swept from V_g = -10 V to V_g = 10 V (forward sweep), minority carriers are attracted to the interface from the bulk of the SiC. Since the concentration of minority carriers is negligible in SiC MOS capacitors, the effect on the characteristics of the trap and de-trap processes at the SiC/SiO_2 interface are not apparent. This implies that the number of trapped charges at the interface is small, suggesting that the value of ΔV_{FB} should remain constant as the temperature changes. However, under negative bias condition, the data show that the value of ΔV_{FB} becomes negative with increasing temperature and whilst both samples show similar behaviour, the changes in ΔV_{FB} for the phosphorus doped dielectric are more noticeable. Meanwhile, under positive bias stress, different trends were observed. ΔV_{FB} remains constant as the temperature increases for undoped samples but the data show that the value of ΔV_{FB} for phosphorus doped samples becomes noticeably positive with increasing temperature. When the gate voltage was swept from V_g = 10V to V_g = -10V (reverse sweep), majority carriers are accumulated at the interface. Since the majority carrier concentration is significantly higher than the minority carrier concentration in SiC MOS capacitors, the effect of trapping and de-trapping due to states at the interface is more obvious for both bias conditions, especially for the phosphorus doped SiO_2 dielectric. The larger changes in ΔV_{FB} for this sweep direction (reverse sweep) can be explained by the trapping of these additional carriers at the interface. The charges trapped under accumulation condition are electrons (negatively charged), hence, the characteristics are shifted to the positive direction.

The data in Fig. 3.5 show the bidirectional characteristics of ΔV_{FB} values for the phosphorus



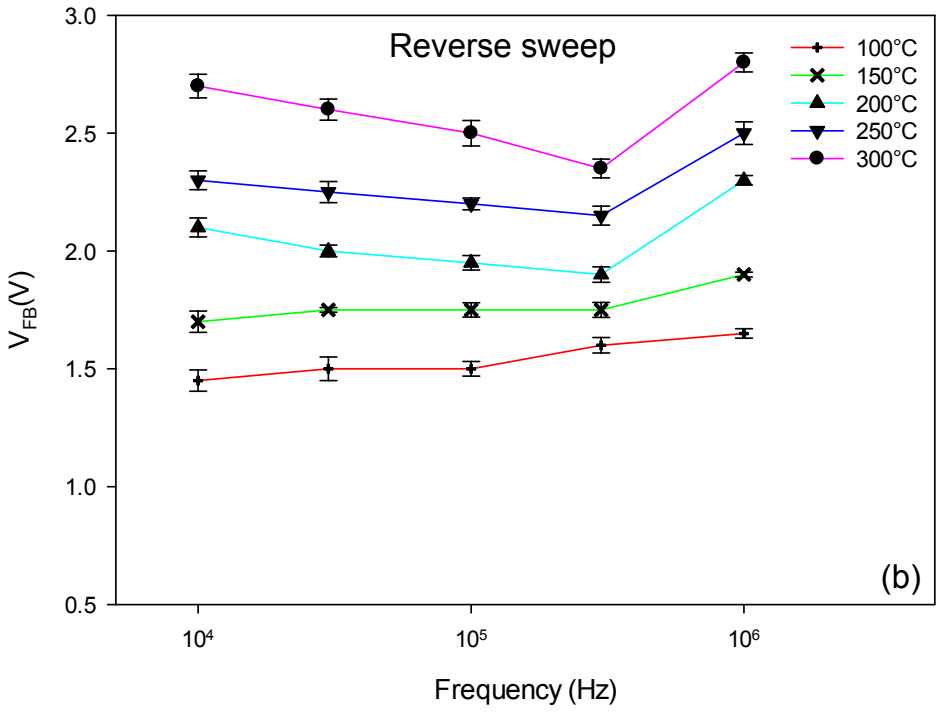


Figure 3.5: Frequency dependence of V_{FB} for the phosphorus doped oxide measured for both directions. Forward sweep Figure (a) and reverse sweep Figure (b).

incorporated sample measured at different frequencies. The data for the forward sweep measurement, at temperatures below 200°C, show a minor variation in ΔV_{FB} with frequency,

but as the temperature is increased above 200°C, the ΔV_{FB} values are significantly reduced with increasing frequency. For reverse sweep measurements, the data show that the shift in ΔV_{FB} is unaffected by frequency, but are shifted to larger ΔV_{FB} as the temperatures are increased, similar to the data shown in Fig. 3.4.

3.1.4 Threshold voltage, V_{TH} instability

The threshold voltage, V_{TH}, is the bias at which the surface potential, Φ_{S}, equals twice the bulk potential Φ_{B} and can be calculated from the C-V characteristics using Eq 3.6. The calculated values are shown by the data in Fig. 3.6. Similar to the data shown in Fig. 3.4, the effect of trapping and de-trapping processes are less significant during the forward sweep, resulting in a smaller shift in V_{TH} as the temperature increases. Furthermore, the threshold voltage shift in the device with the phosphorus doped dielectric is greater (up to 2 V shift at 300°C) than for the undoped dielectric as the temperature increases during reverse sweep for both bias conditions.

The variation in V_{TH} with frequency and temperature was also investigated. The data in Fig. 3.7 show the bidirectional characteristic of V_{TH} for the phosphorus incorporated sample as a function of frequency at elevated temperatures. The same trend is observed for V_{TH} as for V_{FB}, where the instability is more pronounced at 250°C and 300°C. The results show that V_{TH} is stable with frequency when the gate bias is swept from V_g = 10 V to $V_g = -10$ V. However the observed frequency dispersion increases with temperature, similar to the trend observed for the V_{FB} data. At higher temperatures, V_{TH} values decrease because the emission of trapped charges increases as the bandgap of SiC reduces, so a lower bias is required to form an inversion region [42]. From the data, it is clear that the concentration of trapped charge is greater in the phosphorus doped dielectric, than the undoped samples. The enhanced shift in both flatband and threshold voltages are also linked to the presence of a defect arising from the incorporation of positive phosphorus ions in the oxide and at the SiO_2/SiC interface [152–155]. P atoms are not mobile if they are in the form of PSG, formed during the annealing process. PSG is a polar material and the effect of polarization is more significant when it is electrically biased at high temperatures [4, 156]. Different types of voltage stress measurements are needed to investigate the characteristics of NITs [42].

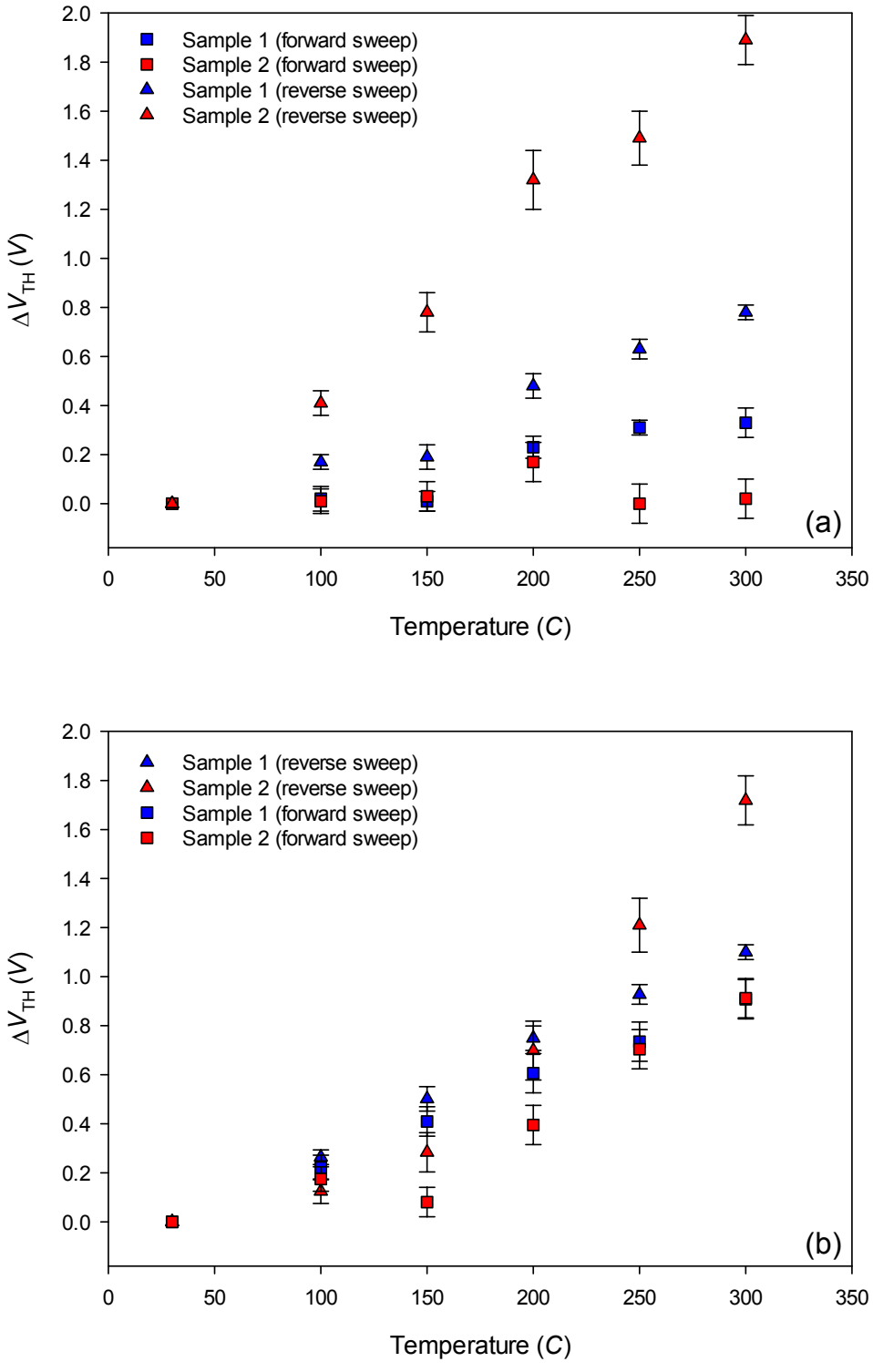


Figure 3.6: Threshold voltage (ΔV_{TH}) extracted from 1 MHz C-V characteristics as a function of temperature for the undoped (sample 1) and phosphorus doped (sample 2) dielectrics under (a) negative and (b) positive gate bias conditions.

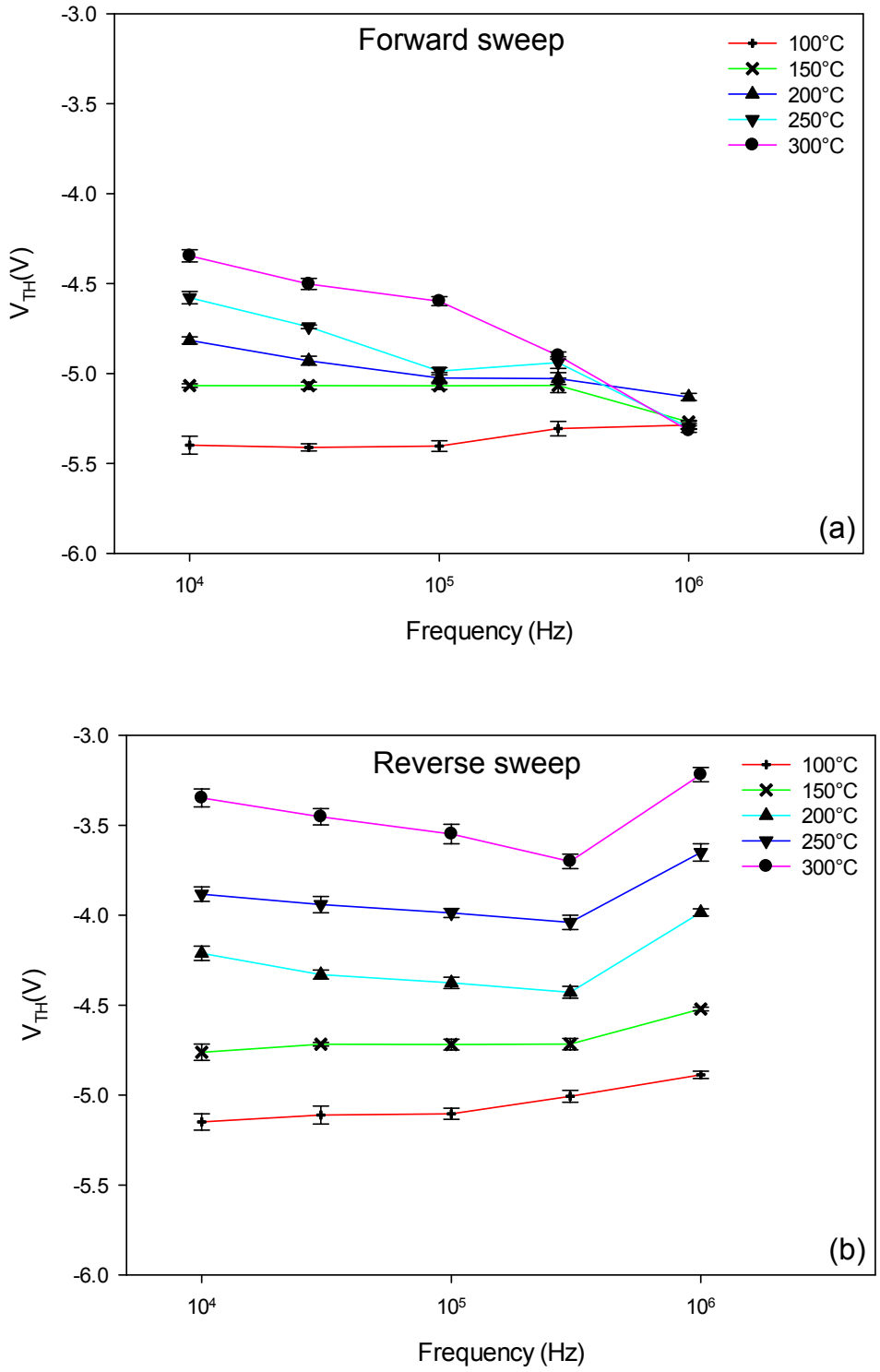


Figure 3.7: Frequency dependence of V_{TH} for sample 2 measured for both directions. Forward sweep figure (a) and reverse sweep figure (b).

3.1.5 Total effective oxide charge density, N_{EFF} in phosphorus incorporated oxide

N_{EFF} depends on the quality of both the gate oxide and interface. Previous studies have examined a range of approaches to reduce N_{EFF}, because it is one of the dominant factors

in the suppression of channel mobility and reduces the quality of oxide based passivation layers [150]. In this study, bidirectional 1 MHz C-V characterization at elevated temperatures was used to compare the temperature dependence of N_{EFF} in the phosphorus incorporated and undoped oxides. N_{EFF} was determined using Eq 3.5, with a work function difference between the aluminium contact and the SiC of 1.0 eV [114]. Fig. 3.8 depicts the dependence of N_{EFF} at elevated temperatures extracted from sweeps forward and reverse for both dielectrics under negative (a) and positive (b) gate bias conditions. For the undoped oxide, the variation in effective oxide charge density shows minor variation with temperature, with values between -2 and -4×10^{11} cm^{-2} in both directions regardless of the applied bias stress. In contrast, under negative bias condition, the data for the forward sweep on the phosphorus doped dielectric show N_{EFF} monotonically decreasing from -2.4×10^{11} cm^{-2} to -6.4×10^{10} cm^{-2} with increasing temperature up to 250°C, before changing polarity to 4.0×10^{9} cm^{-2} at 300°C, but the N_{EFF} increases slowly with increasing temperatures under positive bias condition. In the reverse sweep, significantly different characteristics were observed (both bias conditions). N_{EFF} increases slowly from room temperature to 100°C, followed by an abrupt increase above 100°C. This behaviour may be attributed to the concentration of mobile charge in the phosphorus incorporated oxide, which is distinct from the chemically bonded P atoms that lead to the observed increase in N_{EFF}. This instability in N_{EFF} has two potential origins; charge trapped in the bulk of the dielectric, which is described using an effective charge density (N_{EFF}) and charge trapped in interface states, described using the interface state density (D_{it}). The data in Fig. 3.8 show that the effective charge density in the phosphorus doped dielectric shifts significantly in comparison to the undoped dielectric. From these data it appears that traps in the oxide results in the electrical instability through the capture and emission of electrons and holes [42].

3.1.6 Bias Temperature Stress (BTS)

In order to investigate the presence of mobile charge in these two samples, positive and negative bias temperature stress (BTS) measurements has been performed according to the method described in [151]. Initial C-V measurements at room temperature are taken as a reference (before stress) for both samples. Then, the samples are heated to 200°C and a gate bias to produce an oxide field of around 1 MV/cm is applied for 5 minutes for the charge to drift to the oxide interface. (In this case, the thickness of oxides are around 36 nm, so 3.6 V was applied). The samples are then cooled to room temperature under bias and the C-V measurements are

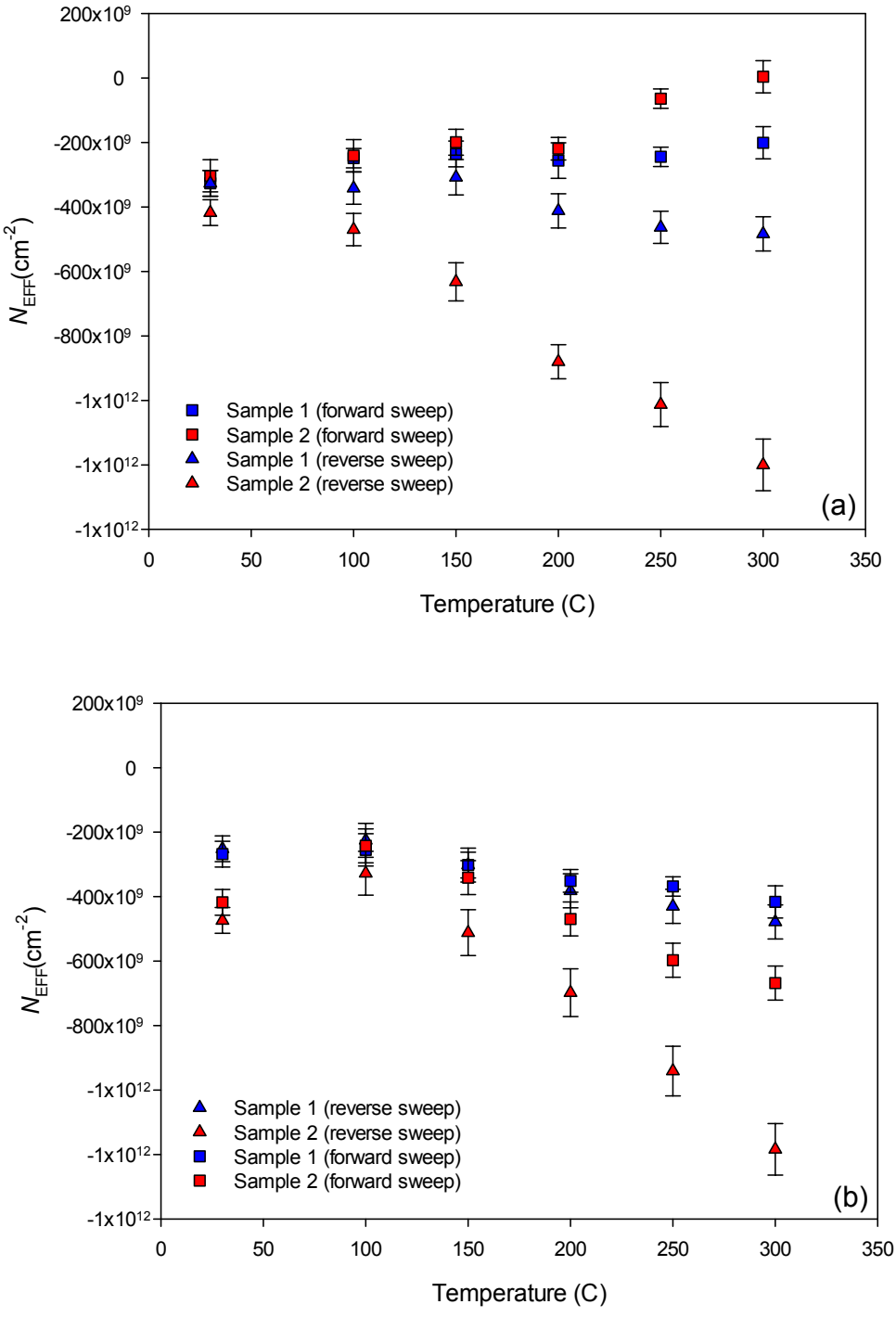


Figure 3.8: Variation in effective oxide charge density in sample 1 and 2 under negative (a) and positive (b) gate bias conditions.

performed. For the negative bias temperature stress (NBTS), the procedure is then repeated with the opposite bias polarity. It is important to keep the oxide field around 1 MV/cm to cause mobile charge to drift and to prevent any charge injection from happening [151]. The flatband voltage shift can be used to determine the mobile charge density. Fresh samples were used for

each test in this experiment.

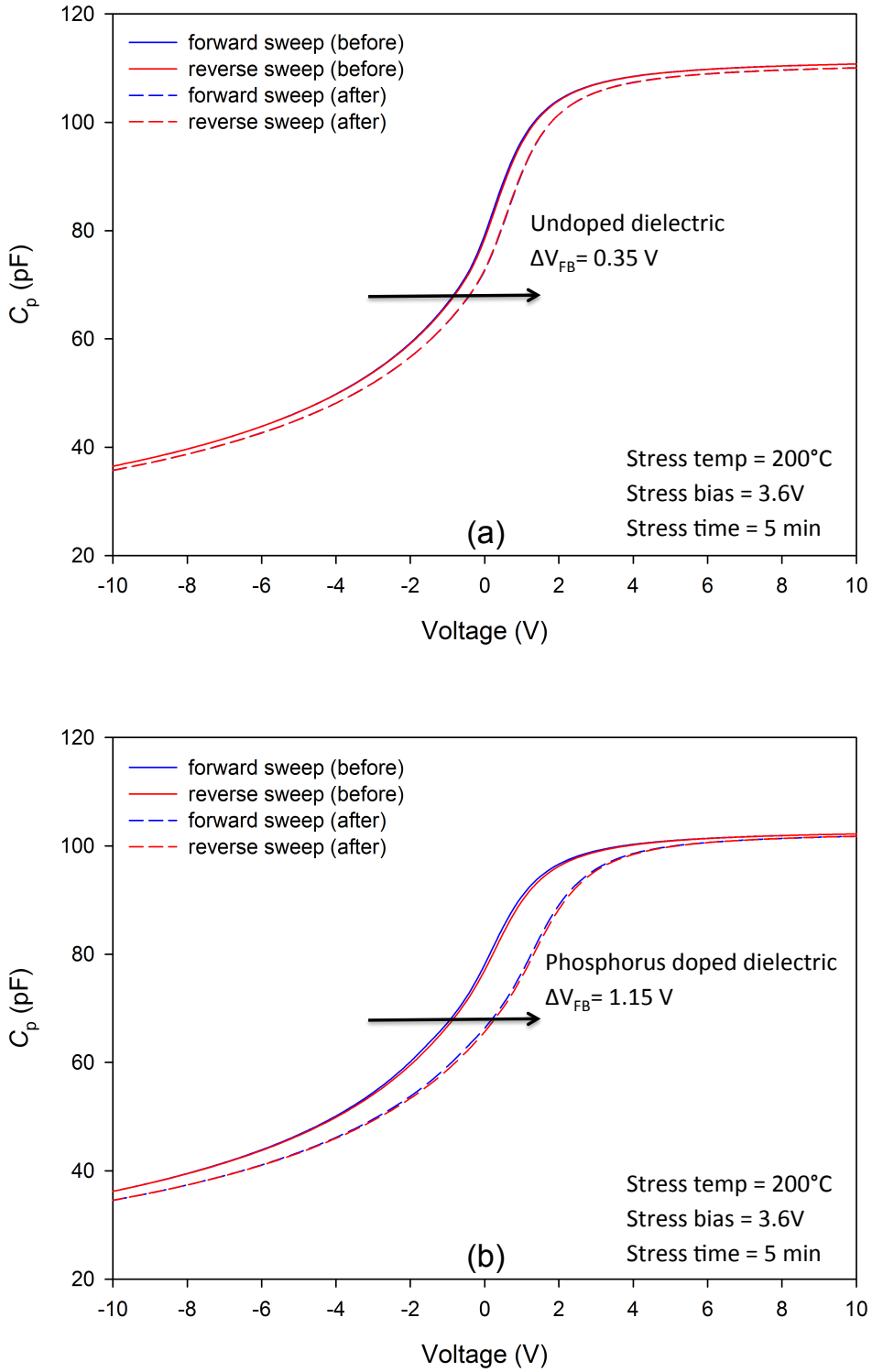


Figure 3.9: C-V curves illustrating the effect of mobile charge motion for undoped (a) and phosphorus doped dielectric (b) measured before (solid lines) and after (dash lines) PBTS.

The data in Fig. 3.9 show the C-V characteristics before and after positive bias temperature

stress (PBTS) for both undoped dielectric (Fig. 3.9a) and phosphorus doped dielectric (Fig. 3.9 b). The undoped samples and phosphorus doped samples indicates V_{FB} shift (different before and after PBTS) of 0.35 V (-3.88×10^{-11} cm^{-2}) and 1.15 V (1.18×10^{-11} cm^{-2}) respectively with almost no hysteresis is seen for forward and reverse sweep for both samples before and after PBTS. These results show that the amount of mobile charge concentration in the phosphorus doped samples is significantly higher than the undoped counterpart, probably due to the mobile ion gettering capability of phosphorus [23, 157]. Positive BTS results obtained here also can be explained by electron trapping at the interface when positive stress has been applied at 200°C before C-V measurements have been performed. As mentioned before, a lot of electrons are trapped at the interface when the positive bias was applied to the gate for 5 minutes, causing the flatband voltage to shift to the positive direction [158, 159].

The results for negative bias temperature stress (NBTS) are shown in Fig. 3.10 for both samples. The C-V characteristics of the undoped sample are very stable; with no hysteresis observed for forward and reverse sweep before and after stress which indicates the absence of mobile charge in the dielectric. In contrast, a small flatband voltage shift, 0.3 V (3.08×10^{-11} cm^{-2}) to the negative direction is observed for the phosphorus doped samples. When the negative bias is applied to the gate for 5 minutes at 200°C, minority carrier (holes) are attracted to the interface and get trapped. However, since holes are minority carriers, the flatband voltage shift after the stress is low in comparison to the shift caused by majority carriers. The trends obtained from BTS shown that the mobile charge has caused the instability to the phosphorus doped samples [160, 161]. These features for electron traps in the oxide are consistent with the results obtained in previous sections (Flatband voltage, V_{FB} instability and Threshold voltage, V_{TH} instability) and agree with observations published elsewhere [158, 159].

3.1.7 Interface Trap Density, D_{it}

Until now the origin of interface traps remains unclear. According to previous reports in the literature, interface traps can be associated with (1) carbon or silicon clusters at the SiC/SiO_2 interface, (2) intrinsic defects formed in the bulk of gate dielectric and (3) interfacial defects at the SiC/SiO_2 interface. Reports also correlate the presence of a carbon defect in the bulk SiC as being responsible for the low quality of gate oxide and increased D_{it} [162]. By incorporating phosphorus, the carbon defects at the SiC/SiO_2 interface can be replaced by P or P=O [163]. Interface state density is known to play an important role in inversion layer mobility and hence the characteristics of the MOSFET. The density of interface traps at the SiC/SiO_2 interface

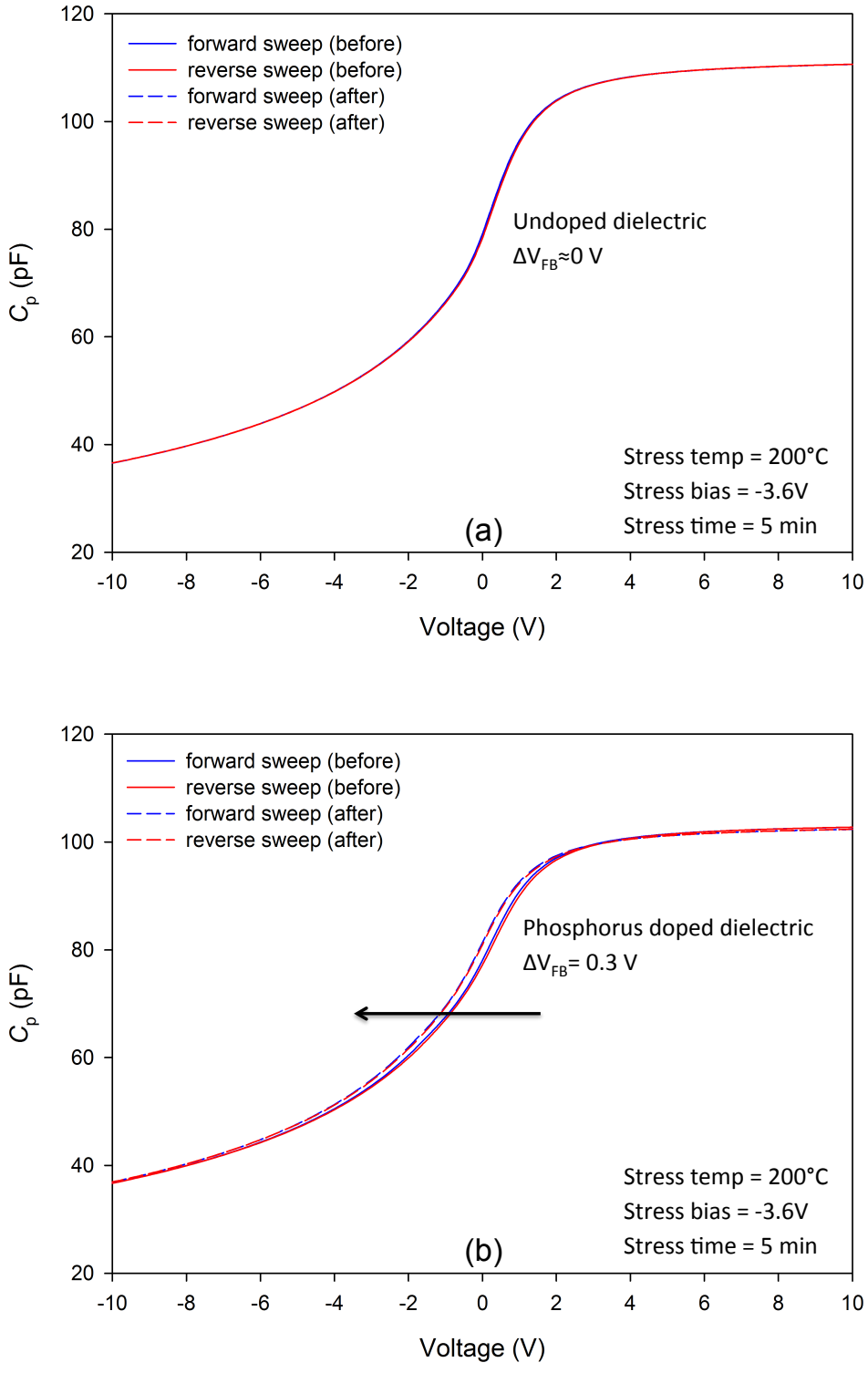


Figure 3.10: C-V curves illustrating the effect of mobile charge motion for undoped (a) and phosphorus doped dielectric (b) measured before (solid lines) and after (dash lines) NBTS.

is higher than at the Si/SiO_2 equivalent and this is often considered to be the primary reason for low mobility [164]. Many researchers reported that mobility can be increased by reducing

$D_{\rm it}$ [4, 50, 141]; however the relation between $D_{\rm it}$ and mobility is still not fully understood. The data in Fig. 3.11 show $D_{\rm it}$ extracted for both samples using the C-ψ_s technique from room temperature quasi-static C-V measurements [121]. It is worth noting that, the value of $D_{\rm it}$ is high in comparison to previously published data because the C-ψ_s technique can accurately determine the contribution of fast states, which are not accurately reflected in the more commonly used Terman or High–Low method [4, 146]. The voltage was swept from depletion to accumulation at a rate of 0.1V/s. A reduction can be observed in the value of $D_{\rm it}$ at $E_c - E$ = 0.2 eV (close to the conduction band) for the phosphorus doped oxide in comparison to the undoped dielectric (sample 1). However, the $D_{\rm it}$ values for sample 2 decreases more slowly as the energy from the conduction band edge increases in comparison to the undoped oxide. Near the conduction band, in the range where $E_c - E$ is between 0.2 to 0.28 eV, the $D_{\rm it}$ of the phosphorus incorporated dielectric is lower; however once $E_c - E > 0.3$ eV, the $D_{\rm it}$ of the undoped sample is lower and decreases more rapidly with energy. This is due to the effect of $D_{\rm it}$ reduction in phosphorus incorporated oxide is not significant for Si face 4H SiC epilayers and the level of phosphorus incorporated in to the oxide is insufficient to form PSG in these samples [60]. However, the results are comparable with those in previously published

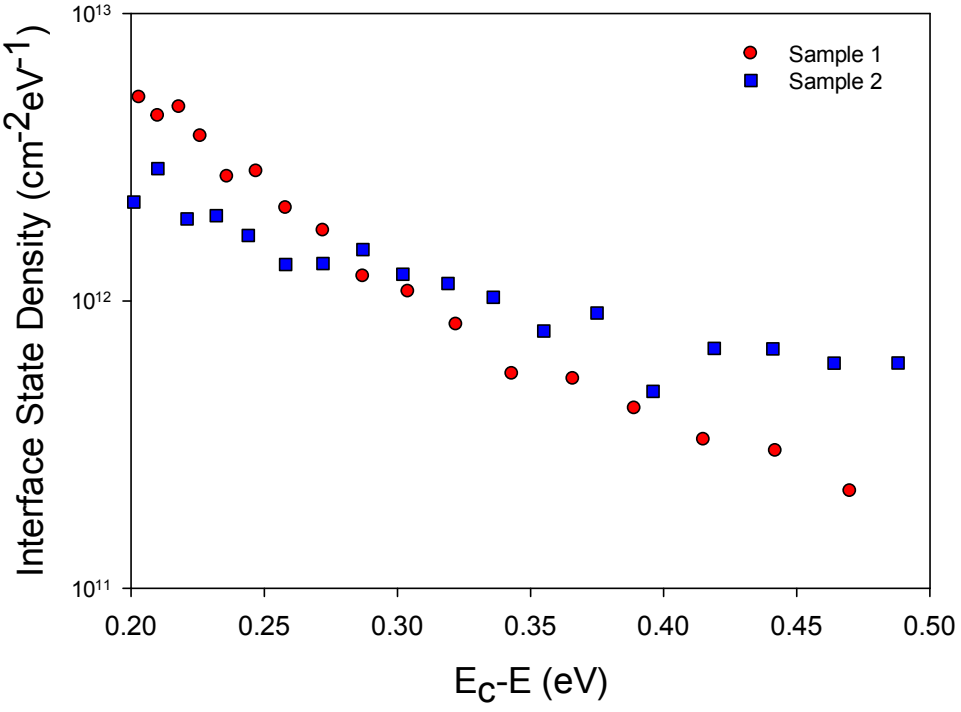


Figure 3.11: Comparison of interface state density ($D_{\rm it}$) as a function of energy, extracted using the C-ψ_s technique.

reports which show a reduction of $D_{\rm it}$ to 2×10^{12} cm^{-2} at 0.2 eV below the conduction band edge [4, 58].

$D_{\rm it}$ as a function of energy within the bandgap was also extracted across the measured temperature range for both samples using the Terman method [60]. As can be seen from the data in Fig. 3.12, the change in $D_{\rm it}$ close to the band edge as the temperature increases is not consistent for both samples, however a trend at energies defined by $E_c - E > 0.3$ eV can be observed. The extracted $D_{\rm it}$ for both dielectrics reduces with increasing temperature across the measured energy range. This suggests that the interface state density, $D_{\rm it}$ has a temperature dependence and therefore is electrically active at elevated temperatures [165]. At high temperatures, the oscillation of the atoms around their equilibrium position, which results in the replacement of the sharply defined energy level for the capture or emission of carriers with a probability density at the specific energy. This results in an increase in the occupancy of traps with carriers that have a sufficiently high energy to enable a capture/emission process [166]. These results can also be explained by correlating the existence of slow and fast interface states that have different time constants that only begin to interact with semiconductor carriers at high temperatures [167], which is in agreement with observation of the SiO_2/SiC interface annealed in nitrogen rich environments [52].

3.2 Positive flatband voltage shift in phosphorus doped N-type 4H-SiC MOS capacitors under constant voltage stressing, (CVS)

Silicon carbide is recognised as being the material of choice for high power, high temperature electronic sensors and circuits because of the superlative material properties, including the high critical breakdown field and wide bandgap [6]. SiC MOSFETs suffer from low channel mobility, which for low gate bias conditions is determined by the high density of interface states ($D_{\rm it}$) present at the SiC/SiO_2 interface [164, 168]. A significant level of research has been undertaken to characterise, understand the origin of and then reduce the value of $D_{\rm it}$ in order to enhance the channel mobility. In contrast to silicon technology, hydrogen annealing has not been shown to reduce $D_{\rm it}$ and current research has suggested the growth of extremely thin oxide layers grown at very high temperatures [35] or nitridation [58] results in an enhancement in carrier mobility, related to the reduction in $D_{\rm it}$ [169]. Additionally, the high concentration of trapping states at the silicon carbide-silicon dioxide interface is linked to the bias temperature instability observed in SiC MOSFETs owing to thermal detrapping of electrons at high temperatures [57, 99, 125].

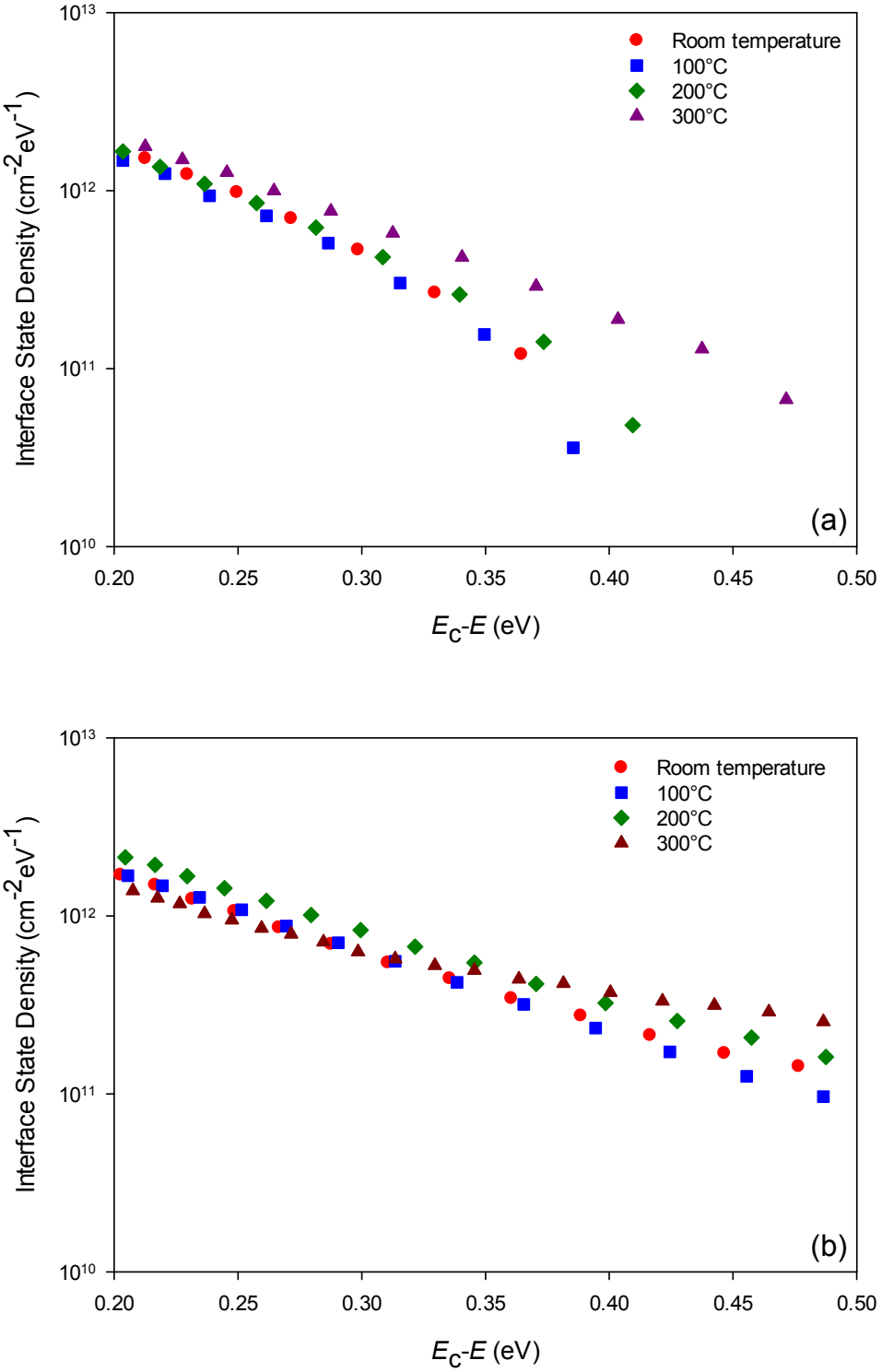


Figure 3.12: Interface state density (D_{it}) as a function of energy at varying temperatures extracted using Terman method for sample1 (a) and sample 2 (b).

It has been shown that the incorporation of sodium into the gate oxide dramatically increases the field effect mobility of MOSFETs by reducing the surface electric field [43, 80]. Unfortunately, the device is unstable in terms of threshold voltage, V_{TH} when operated at high temperatures due to the presence of mobile charge in the oxide. The mobile charge densities are in the range of 10^{11} to 10^{13} cm^{-2}, which results in significant hysteresis in the C-V characteristics, and resulting in the observed threshold instability, especially at high temperatures [59]. The presence of carbon in 4H-SiC results in a more complicated oxidation chemistry than that of silicon. For example, the oxidation of 4H-SiC is very slow [170] in comparison to silicon and the generation of defects in the oxide and at the interface are inevitable [38]. The belief that minimizing SiC oxidation, thus reducing carbon impurity at the interface has led to the idea of forming an ultra-thin SiO_2 interfacial layer between the SiC and subsequent high-κ dielectric layers. The gate stack of SiC/SiO_2/Al_2O_3 has successfully increased the field effect mobility up to 300 cm^2/V.s in MOSFETs. However, V_{TH} typically reduces becoming zero as the peak mobility increases. There are also a number of reports using alternative high-κ materials including La_2O_3 [90, 92], HfO_2 [171, 172] and Si_3N_4 [93] as a gate dielectrics.

Post oxide annealing (POA) [65, 173] has been confirmed to reduce $D_{\rm it}$, and hence increase the channel mobility of MOSFETs. The most effective POA of a SiO_2 gate dielectric is by incorporating phosphorus at the interface, which has been shown to enhance the mobility, resulting in values up to 89 cm^2/Vs [2]; however, the long term stability of $V_{\rm FB}$ in phosphorus doped MOS capacitors at high temperatures is still unresolved. The incorporation of phosphorus into SiO_2 changes the gate dielectric into phospho-silicate glass (PSG). In Si technology, a very thin PSG film has been used between the metal gate and SiO_2 layer to reduce the effect of mobile charge (Na^+ ion getter), stabilising the device characteristics. Besides, the improvement in charge stability and breakdown voltage of phosphorus doped SiO_2/Si MOS devices can be realised by a modification technique reported by [174], where the characteristics of Si MOS devices are modified by electron injection at high electric field.

Phosphorus doped silicon glass (PSG) is commonly used in the manufacture of semiconductor devices. A number of extensive studies have been published on the defect structure of the bulk material [61, 153, 174]. However, relatively little is known about the trapping characteristics of phosphorus-doped SiO_2/ 4H-SiC MOS capacitors [59]. The instability of the flatband voltage in phosphorus incorporated 4H-SiC MOS capacitors due to the high concentration of defects at the interface and in the bulk oxide is a major concern, even at room temperature. This affects the device characteristics when measured under different gate bias conditions and results in

variation of the extracted parameters. It has been suggested that the origin of the flatband shift is due to charge injection from the SiC substrate into the oxide [160]. Recently, mobile charge has been detected by triangular voltage sweep (TVS) measurements and this has been identified as the cause of the instability of SiC MOS at elevated temperatures [175]. Nevertheless, the intrinsic mobile charge in the as-oxidized SiC MOS capacitors can be reduced or increased by means of the post-oxide annealing treatment [160].

The stability of phosphorus-doped SiO_2 gate dielectrics are determined by observing the effect of high electric field and bias stress time on the device characteristics. In particular, the shift in flatband voltage, effective oxide charge, interface state density and the electron conduction mechanism have been investigated at room and elevated temperatures. Direct comparisons to the conventional thermal oxide gate dielectric sample were made in order to determine the origin of flatband shift in phosphorus-doped SiO_2 devices which is necessary for the development of stable and reliable 4H-SiC MOS devices.

3.2.1 Experimental

Two 100 mm, Si-face, 4° off axis, 4H-SiC n^+ wafers with an epitaxial layer doped with nitrogen at a concentration of 1×10^{17} cm^{-3} were used to fabricate MOS capacitors. Oxide films on both samples were fabricated by thermal oxidation, followed by post oxidation annealing. Then, a nitride cap was deposited to give an effective oxide thickness of 33 nm. For sample 2 (phosphorus-doped SiO_2 devices), one extra step was added to produce phosphosilicate glass (PSG) oxide where the gate dielectric was annealed in a phosphorus rich environment (planar source of phosphorus pentoxide, P_2O_5) prior to metallisation. After aluminium gate deposition, both samples underwent post metallisation annealing (PMA) to minimise the effects of high temperature measurements on the characteristics. NMOS capacitors with photolithographically defined areas of 1.12×10^5 μm^2 were characterised using a Keithley 4200 parameter analyser.

A range of gate bias conditions and bias stress times have been applied to observe the characteristics of phosphorus-doped SiO_2 devices. First, the capacitors were held with different bias stress times (0s to 999s) and bidirectional 1 MHz C-V measurements from accumulation (V_g =10 V) to deep depletion ($V_g = -10$ V) were performed at room temperature and at 250°C. Furthermore, the same bidirectional measurements were repeated but with different starting gate voltages of 10, 20 and 30 V and -10, -20 and -30 V for reverse sweep and forward

sweep respectively at room temperature. Finally, the capacitors were held with different stress time at high electric field, -30 V for forward sweep and 30 V for reverse sweep. The effect of bias voltage and stress time (under the condition of Fowler-Nordheim injection which results in electron trapping in the bulk of the oxide) on the phosphorus doped SiO_2 were investigated from the changes in flatband voltage, ΔV_{FB} (with respect to data from the first measurement) effective oxide charge, ΔN_{EFF} and interface state density, ΔD_{it}. The undoped SiO_2 MOS capacitors samples were used as a comparison. Fresh samples were used for each measurement to prevent the effect of charge accumulation in traps while analysing the data.

3.2.2 Results

Under low to medium bias region, the gate leakage current is dominated by the PF emission and the TAT mechanisms. PF emission is the electric field-enhanced thermal emission of electrons from a trap state to the continuum states associated with a conductive dislocation. TAT is the other trap-assisted transport mechanism which becomes significant in the vicinity of zero gate bias to compensate the non-zero PF current at this bias. In this process, electrons tunnel from metal to semiconductor through a band of localized traps.

When a large positive voltage is applied to the metal with respect to the substrate, the band diagram of metal is lowered, and tunnelling of electrons from the conduction band of the semiconductor into the conduction band of the oxide, through an approximately triangular barrier can occur, as shown in Fig 3.13. This kind of tunnelling through a triangular potential barrier is known as Fowler-Nordheim tunnelling [176]. Fowler-Nordheim plots are a useful method to determine the relation between the strength of electric field and barrier height at the interface. The data in Fig 3.15 show FN-plots ((ln(J/E^2) verses inverse electric field (1/E)) for both samples (a) at room temperature and (b) 100°C. FN tunnelling of electrons can be expressed as

$$J_{FN} = AE_{\mathrm{OX}}^2 exp\left(\frac{-B}{E_{\mathrm{OX}}}\right) \tag{3.10}$$

where J is the current density, E the oxide field, and the pre-exponent A and slope B are given by

$$A = \frac{q^3}{16\pi^2\hbar\phi_{\mathrm{B}}}\left(\frac{m}{m_{\mathrm{OX}}}\right) = 1.54\times10^{-6}\left(\frac{m}{m_{\mathrm{OX}}}\right)\frac{1}{\phi_{\mathrm{B}}}[A/V^2] \tag{3.11}$$

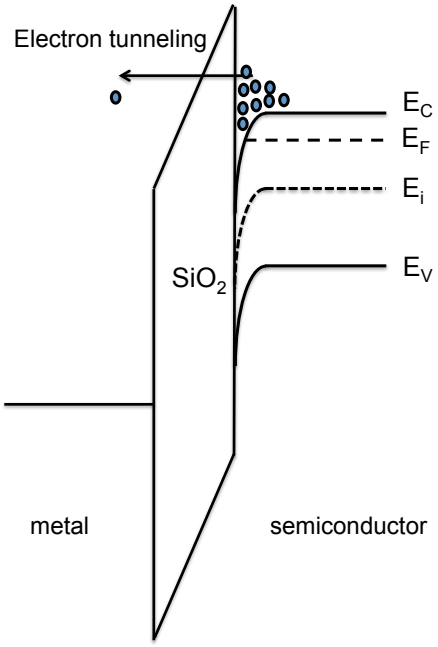


Figure 3.13: Electrons injection into the oxide by means of FN tunneling under high electric field. (Accumulation region for n-type MOS capacitor)

$$B = \frac{4\pi\sqrt{2m_{\mathrm{OX}}\phi_B^3}}{3q\hbar} = 6.83 \times 10^7 \sqrt{\frac{m_{\mathrm{OX}}\phi_B^3}{m}}[V/cm] \tag{3.12}$$

where q is the electron charge, m the free electron mass, m_{OX} the electron mass in oxide, $\hbar$ the Planck's reduced constant and ϕ_{B} the barrier height in electron volts. This equation can be applied to both polarities. This model is assumed to be valid both for strong accumulation and strong inversion corresponding to non-degenerate n-and p-type substrates respectively [177]. In this work, electrons are injected from the semiconductor to the oxide because the measurements were performed under positive polarity which is an accumulation region of n-type MOS capacitor [178].

Quantum mechanical tunnelling describes the movement of carriers through a classically forbidden energy state. Fig 3.14 shows the gate current characteristics as a function of gate bias for both samples measured at room temperature and 100°C under positive bias (accumulation region for n-type MOS capacitor). For the undoped SiO_2 samples, the I-V curves are consistent on the first, second and third measurements. But for phosphorus-doped SiO_2 the J-E curves are shifted to the positive every time the measurement is repeated. The accumulation of negative charge in the gate dielectric shifts the J-E curves in the positive direction and increases the breakdown voltage by changing the charge state of the defect [179]. This effect can be explained by improving of weak spots through the accumulation of a negative charge in

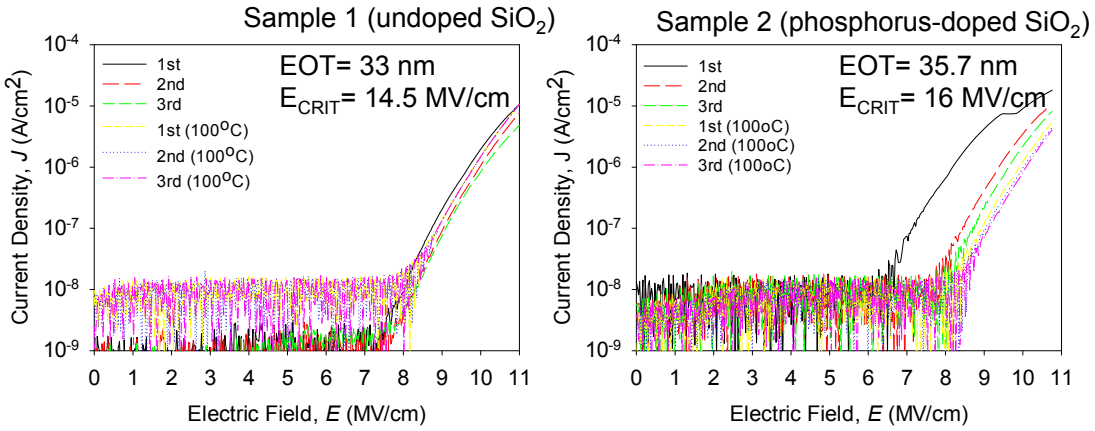


Figure 3.14: J-E characteristics of sample 1 and sample 2 at room temperature and 100°C under positive bias (accumulation region for n-type MOS capacitor).

the gate dielectric. As the result, the barrier height at the interface increases, thus improves the breakdown voltage.

The barrier height, ϕ_{B} for both samples can be extracted from the FN slopes, B (Equation 3.12), using the effective electron mass, m_e=0.42 m_0 [180, 181]. Due to the quatization effect in the accumulation layer and image force lowering, the extracted values of ϕ_{B} approximately 0.3 eV lower than those obtained by internal photoemission experiments [182]. The interface state density which enhanced the electron trapping and oxide degradation not only affects the channel mobility, but also influences the barrier height by acting as a primary source for FN tunnelling [183]. The data show that the two samples exhibit different temperature dependences. The $\ln(J/E^2)$ values increase as the temperature was increased to 100°C for undoped samples but the opposite trend was observed for phosphorus-doped SiO_2. This indicates the leakage current of the undoped samples increased at 100°C which can be correlated to the lower breakdown voltage with the increase in temperature. In contrast, the breakdown voltage of the phosphorus-doped SiO_2 device increased with temperature. At 100°C, the electron traps make a major contribution to the value of the accumulated negative charge in the oxide, resulting in an increased potential barrier. The accumulation of a negative charge in the PSG film leads to an increase in the energy barrier [181] at the injection interface boundary, increasing the breakdown voltage of the gate dielectric. This phenomena is more significant for phosphorus-doped SiO_2 due to the existence of phosphorus atoms that enhance the electrons injection into the gate dielectric [4, 59, 174].

The data presented in Fig 3.16 are the shifts in the flatband voltage, ΔV_{FB} and effective oxide charge density, ΔN_{EFF} as a function of gate bias stress time from the CVS experiment. The

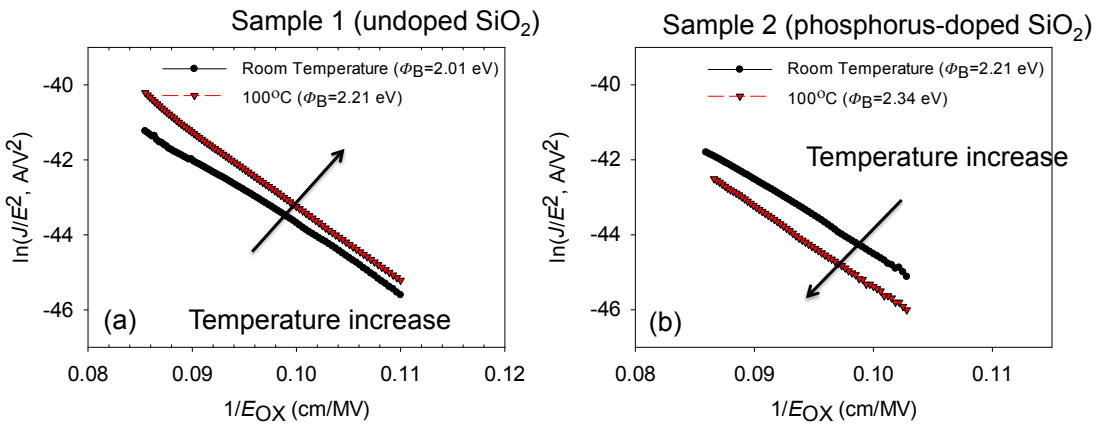


Figure 3.15: FN plots of (a) undoped and (b) phosphorus-doped SiO_2 samples at room temperature and 100°C.

data show the difference in sweep direction from a starting bias of $\pm$ 10 V measured at room temperature (Figs 3.16 (a) and (b)) and at 250°C (Figs 3.16 (c) and (d)). Under forward sweep, the shift in flatband voltage, $\Delta V_{\rm FB}$ and effective oxide charge, $\Delta N_{\rm EFF}$ for sample 1 are negligibly small at both room temperature and 250°C for the stress times investigated. The shift for both samples in the forward sweep are also small (less than 0.3 V) at room temperature, as well as at 250°C. However, significant changes in flatband voltage (up to 0.7 V at 999 s) and effective oxide charge (up to -7×10^{11} cm^{-2}) are observed for the phosphorus-doped sample (sample 2) under reverse sweep conditions at room temperature as the bias stress time is increased. The shifts for the phosphorus-doped samples for both flatband voltage and effective oxide charge become more apparent at 250°C under reverse sweep conditions, where the flatband voltages increase rapidly ($\Delta V_{\rm FB}$= 2.3 V) for stress times between 0 and 200 s, before starting to saturate at approximately 2.5 V after 500 s. The same trends were observed for the effective oxide charge with increasing bias stress time at 250°C. First order electron trapping kinetic can be used to extract the trap charge concentration, $N_{\rm OT}$ and effective capture cross-section, $\sigma_{\rm n}$ [184, 185]. The first order electron trapping can be given as

$$V_{\rm FB}(t) = \Delta V_{\rm FB0}\,[1 - \exp(-t/\tau)] \tag{3.13}$$

where τ is the trapping time, τ=1/(σJ) and J is the flux density of the injected electrons. The fitting result for phosphorus-doped SiO_2 sample suggests that the $N_{\rm OT}$ and $\sigma_{\rm n}$ are approximately in the order 10^{11} cm^{-2} and 10^{-19} cm^2 respectively. The extracted value of $\sigma_{\rm n}$ is smaller in comparison to those reported for silicon (approximately 10^{-15} cm^2 due to the metalic contamination [184, 186, 187] and 10^{-17} cm^2 for the water-related trap [188]) but in

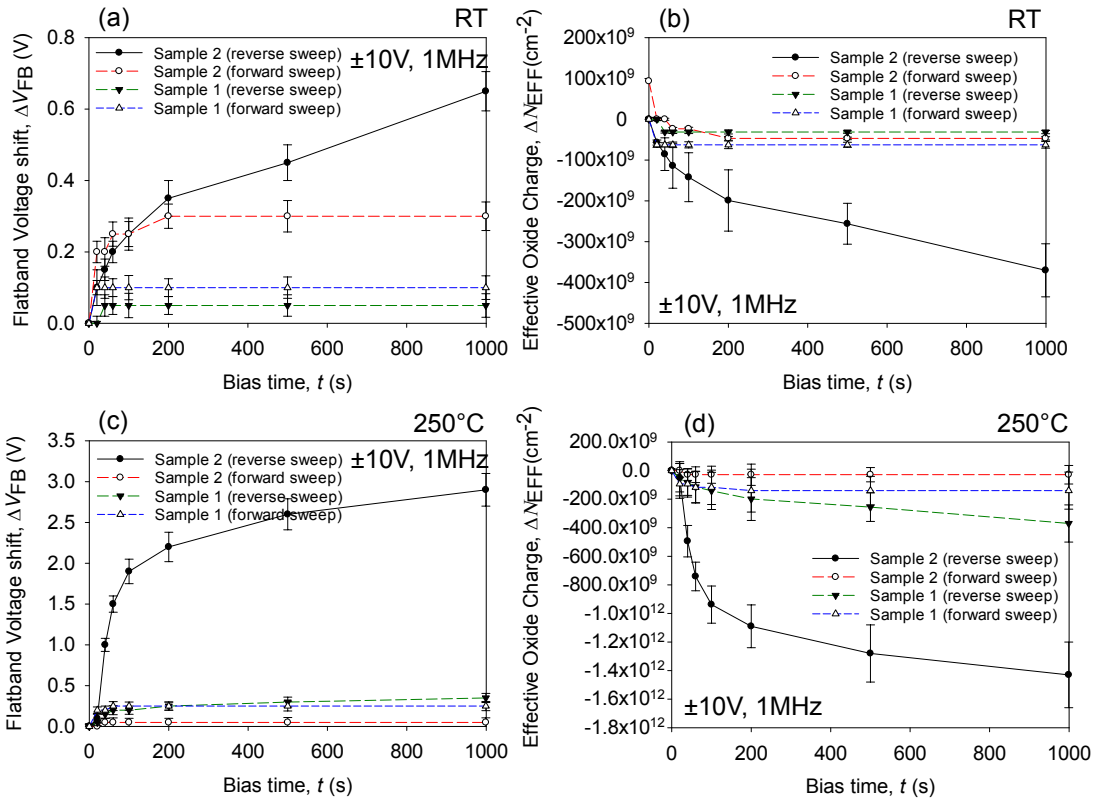


Figure 3.16: Shift in flatband voltage, ΔV_{FB} and effective oxide charge density, ΔN_{EFF} under different gate bias stress times at the room temperature (a and b respectively) and 250°C (c and d respectively) extracted from 1 MHz C-V curves. ΔV_{FB} is defined as the difference of ΔV_{FB} without bias stress time and those ΔV_{FB} obtained at different bias stress time.

agreement with those reported for SiC devices in the literature [37, 81, 189], which is in the range of 10^{-16} to 10^{-22} cm^2 especially for phosphorus-treated 4H-SiC MOS capacitor that lies in the lower 10^{-18} cm^2 range [190]. It has been suggested that small capture cross sections are a combination of midgap interface states and oxide traps, which influencing the long-term device stabilty [189]. As discussed in the previous section (Section 3.1), these results suggest that the instability of phosphorus-doped SiO_2 is due to charge trapping at the interface and in the oxide, resulting in electrons being injected into the bulk oxide, resulting in the increasingly negative effective oxide charge [59].

As reported in the literature [179, 191], the effective oxide charge in MOS capacitors can be modified by the injection of electrons into the gate dielectric, which typically occurs at high electric field. Electron injection from the semiconductor to the gate dielectric or from the gate contact to the gate dielectric is likely at high temperatures via both tunnelling and emission. A tunnelling current occurs when electrons injection occurs through a classically

forbidden energy barrier from conduction band into the oxide bandgap [176]. The consequence of this phenomenon includes increased gate leakage current due to the degradation of the gate dielectric. In SiC, since the interface trap density is high (in comparison to Si), the charge carriers can become trapped, thus permanently changing the characteristic behaviour of the dielectric, resulting in instability in the device characteristics. For phosphorus-doped SiO_2, the carriers traverse the SiC/SiO_2 interface, leading to the accumulation of negative charge in the bulk of the phosphorus-doped gate dielectric, resulting in the shift of the flatband voltage in the positive direction.

In order to investigate the stability and effect of electron injection at different electric fields on the flatband voltage and effective oxide charge, 1 MHz C-V measurements with starting gate bias conditions of -10, -20 and -30 V for forward sweep and 10, 20 and 30 V for reverse sweep were performed. The data in Figs 3.17(a) and (b) show the effect of starting voltage in the C-V characteristics without bias stress time on the stability of flatband voltage and effective oxide charge respectively. As described previously, the changes in both flatband voltage and effective oxide charge are less significant for the characteristics determined from a forward sweep for both samples. Under reverse sweep conditions, the flatband voltage and effective oxide charge in phosphorus doped samples increases with starting voltage. Both flatband voltage shift and changes in effective oxide charge are greater (up to 2.5 V and -1.2×10^{14} cm^{-2} respectively) in comparison to the thermally grown oxide for a starting bias of 30 V.

The data in Figs 3.17 (c) and (d) show the changes in flatband voltage and effective oxide charge as a function of bias stress time when the device was held at -30 V (forward sweep) and 30 V (reverse sweep) respectively. The changes in flatband voltage and effective oxide charge are negligible under forward sweep conditions. Under reverse sweep, the shifts in flatband voltage and effective oxide charge increase with bias stress time for both samples indicating that the charge trapping effect is apparent under the reverse sweep condition.

The positive shifts in C-V characteristics for both samples occur at higher voltages when longer bias stress times were applied. As can be seen from the data in Figs 3.17 (c) and (d), the shift in the flatband voltage and effective oxide charge increased with the bias time, suggesting that there is a limit to the charge density that can be injected. These results are in good agreement with those reported previously for phosphorus doped SiO_2/Si MOS capacitors [174, 179]. Andreev observed that the injected charge density depends on the thickness of the phosphorus-doped oxide, where the accumulated negative charge density increased with increasing phosphorus-doped SiO_2 film thickness. Reports in the literature have

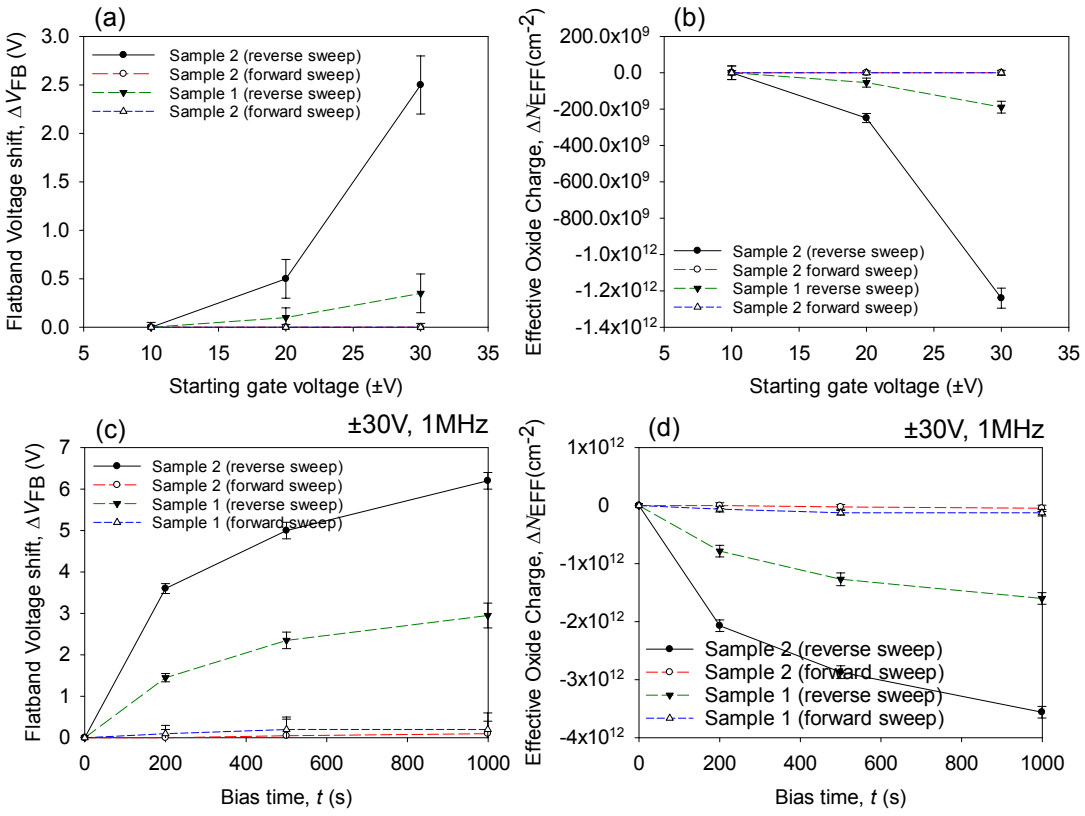


Figure 3.17: Shift in flatband voltage (a) and effective oxide charge density (b) at room temperature under different gate bias conditions. Shift in flatband voltage (c) and effective oxide charge density (d) at high voltage (± 30 V) held with different bias stress time up to 999 s.

also shown that the stability of phosphorus-passivated 4H-SiC MOSFETs can be improved by reducing the thickness of the interfacial PSG gate dielectric layer [42, 58, 60]. In n-type devices, the density of interfacial acceptors is considerably higher than the donor concentration. An increase in the PSG film thickness is unacceptable for thin gate dielectrics, since this leads to excess doping of the SiO_2 film with phosphorus and as a consequence, leads to deterioration in the charge stability in the bulk oxide and at the interface. It has also been reported that an increase in the phosphorus concentration in the PSG film to more than 1.5 % may cause polarisation to the charge exist in the oxide (flatband) and a significant decrease in the charge stability of the gate dielectric [174].

To study the origin of the shift in flatband voltage and effective oxide charge, the interface state density was extracted using the Terman method as a function of bias stress time, as shown by the data in Fig 3.18. Both samples exhibit an increase in interface state density, when the oxide is subjected to a bias (V_g= 30V) for 200 s. The interface state density does not change

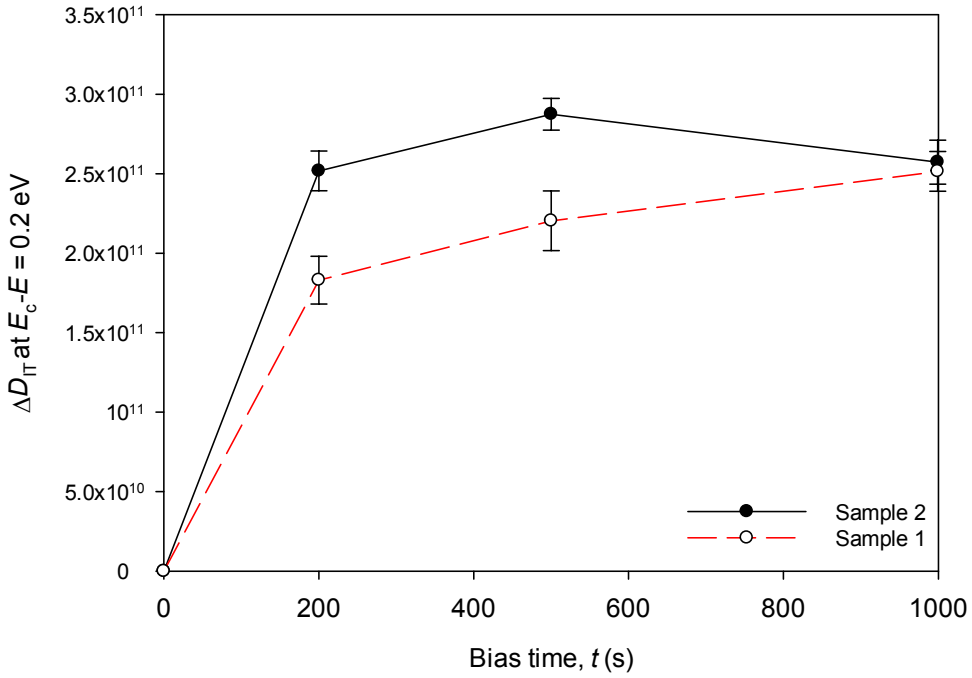


Figure 3.18: The changes of $\Delta D_{\rm it}$ as a function bias stress time for sample 1 and sample 2 under reverse sweep measured from V_g= 30V at room temperature.

significantly for bias stress times $>$ 200 s suggesting that all the available states have been filled. Further increases in $D_{\rm it}$ with bias stress time for the phosphorus-doped SiO_2 device (sample 2) in comparison to the un-doped SiO_2 (sample 1) is one possible origin of the larger positive flatband shift.

3.3 Discussion

Metal contamination such as sodium and potassium have been considered to be the origin of mobile ions in metal-oxide-semiconductor devices. In this study, the influence of mobile ions due to contamination is ruled out because both samples went through the same oxidation process (the contamination level should be identical) allowing the effect of the phosphorus incorporation in oxide to be determined. The results show that the flatband voltages of phosphorus doped SiO_2 are shifted to the positive under reverse sweep as the bias stress time increases at room temperature and the changes are more pronounced at 250°C. Enhanced shifts to the positive are observed when high starting voltages are applied to the capacitors. This phenomenon is more noticeable when high voltage and longer bias stress times are used in

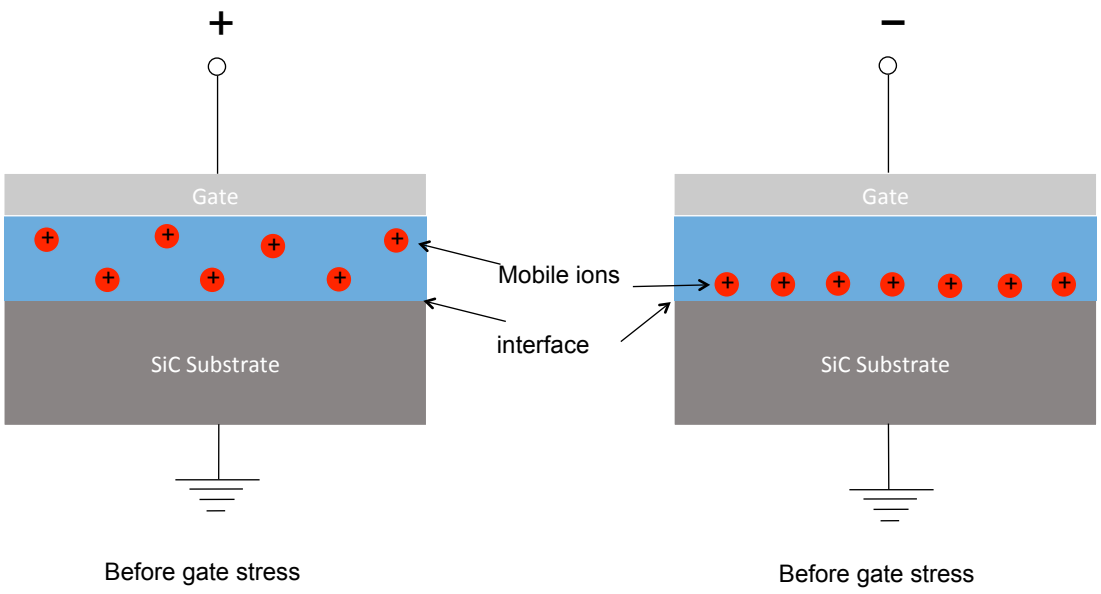


Figure 3.19: Mobile charges are moved to near interface as the constant high voltages are applied with certain bias stress time.

the measurements. Under forward sweep, the flatband voltages are stable and result in a shift that is negligible in comparison to the flatband voltage shift under reverse bias. The possible origin for the positive flatband voltage shifts can be explained by electron injection becoming enhanced with the existence of traps at the interface and increased mobile charge density. As previously reported in [59], the mobile charge density in phosphorus doped SiO_2 is high in comparison to thermally grown oxide, due to the gettering effect that removes undesirable impurities, increasing the quantity of mobile charge [157]. The mobile charge density has been determined from the bias temperature stress, where the mobile ions are able to move at high temperatures. The shift due to the mobile charge can be positive or negative depending on the bias polarity (NBTS or PBTS), but note that NBTS is usually dominated by electron trapping similar to CVS. In constant voltage stress experiment, the data show that the electrons are injected into the oxide even at room temperature when high electric fields are applied for long periods. The trapped charges for electron trapping are negatively charged. Hence, the C-V curve will be shifted to the positive direction. Significant positive shift in flatband voltage is observed for the phosphorus-doped SiO_2 sample due to the high concentration of mobile ions and enhance electron injection into the oxide.

Fig 3.19 is a schematic showing the movement of mobile ions which are the likely cause of the observed positive flatband voltage shift. The positively charged ions exist in the phosphorus doped SiO_2 capture the accumulated electrons injected from the semiconductor

at the interface [179]. When high electric fields were applied at the gate (the barrier height is thinner and more electrons are attracted close to the interface as the Fermi level is in the conduction band), electrons are easily injected into the dielectric, which results in a negatively charged oxide, and so the shift in flatband voltage can be observed [174]. At high temperatures and under high electric field, the mobile charge in the oxide will diffuse to the interface, or away from the interface depending on the polarity of applied bias. The movement of mobile charge is also attributed to the positive shift in the phosphorus doped SiO_2 samples. Thus, in this sense, a strong correlation between the positive shift in flatband voltage and the mobile charge determined by bias temperature stress measurements was identified with 2×10^{11} cm^{-2} and 7×10^{11} cm^{-2} for undoped and phosphorus doped SiO_2 samples respectively. Two main factors that are influencing the shift in the flatband voltage of the phosphorus-doped SiO_2 are mobile-charge (BTS experiment) and electron injection (CVS experiment). First, the flatband voltage shift under BTS, ($<$1MV/cm) is due to the movement of the mobile charge in the oxide. Second, Fowler-Nordheim injection which results in electron trapping in the bulk of the oxide is the factor of the significant flatband voltage shift under high-field stress.

Interface traps can be either acceptor-like or donor-like and the donor-like trap energy levels are located in the lower half of the band-gap. Those trap levels are positively charged if they are empty and electrically neutral when occupied by an electron. The acceptor-like energy levels are located in the upper half of the band-gap. Those trap levels are electrically neutral if there are empty and negatively charged when occupied by an electron. Under positive bias (accumulation), where the majority of electrons are accumulated at the interface, the states in upper half of bandgap become occupied and resulting in the oxide becoming negatively charged. The electrons are increasingly injected from the semiconductor into the oxide under high field conditions as the band bending exposes the defects that lie close to the Fermi level. Injection of electrons into the oxide occurs easily at the SiC/SiO_2 interface because the electric fields in SiC devices are much higher than in silicon and the barrier height at SiC/SiO_2 interface is lower than the barrier height for Si/SiO_2 [183] and this becomes a serious issue as the temperature increases [192]. The increased temperature results in the barrier heights reducing, thus electrons gain sufficient energy to overcome the barrier at the interface and are injected into the dielectric. It has been reported that the injection of electrons into the oxide generates interface states that are not only affecting the channel mobility but also giving influences the barrier height for Fowler-Nordheim tunnelling [181].

3.3.1 Conclusion

The incorporation of phosphorus at the SiO_2/SiC interface results in a reduction in the interface state density near the conduction band and an increase in the instability of V_{FB}, V_{TH}, and N_{EFF} at high temperatures. To date there are limited reports concerning the stability of phosphorus-doped SiO_2 in 4H-SiC at elevated temperatures. In this chapter, the effect of phosphorus incorporation in the gate dielectric was extracted from bidirectional C-V measurements at temperatures up to 300°C. Although the effective oxide charge (N_{EFF}) in phosphorus-doped SiO_2 has been slightly reduced, the instability at high temperatures is a concern. The results from other parameters (V_{FB} and V_{TH}) also showed instability depending on the gate bias, frequency and temperature. In forward sweep, both samples give stable V_{FB} and V_{TH} values even at high temperatures. Meanwhile, in reverse sweep, due to charge trapping, V_{FB} and V_{TH} shifts increase with temperature. The D_{it} of both samples was compared and it was found that phosphorus-doped oxides (sample 2) have slightly lower D_{it} than non doped oxides near the conduction band. In this case, the effect of mobile ions and charge traps at high temperatures should not be neglected. This could cause electron and hole trapping to occur in the gate dielectric and at the SiC interface. The implementation of phosphorus incorporated oxide in SiC is encouraging to improve the channel mobility. However, the stability and reliability aspects are always essential to be taken into consideration in terms of device performance. Therefore, it is important to improve the stability of phosphorus incorporated devices not only at room temperature but also at high temperatures so that the advantageous effect of phosphorus incorporation is not reduced. This work has shown that the inclusion of phosphorus (below 1% levels) in the silicon dioxide gate dielectric of MOSFET structures can be highly beneficial for room temperature performance, the instability of the resulting devices when operated at high temperatures means this technique is not suitable for high temperature circuits.

The incorporation of phosphorus in oxide and at the SiO_2/SiC interface shifts the magnitude of flatband voltage and increases the effective oxide charge. The influence of phosphorus incorporation in the gate dielectric was investigated from C-V measurements at high voltages up to 30 V with bias hold times up to 999 s. In forward sweep, the flatband voltages and effective oxide charges are stable even at high voltage and long bias stress time. However, in reverse sweep, the flatband voltage and effective oxide charges increase significantly especially at a higher starting voltages and for longer bias stress times. This can be attributed to the capture of electrons into the oxide during positive bias stress. The effect becomes more prominent when phosphorus atoms exist at the interface because of the gettering effect that increases the quantity of mobile charge in the oxide. The data also reveal that electron injection is more likely

to occur to phosphorus doped SiO_2, due to the high density of mobile charge in the oxide and this leads to instability in C-V characteristics, especially at high temperatures. The presence of P atoms in the oxide results in a greater concentration of mobile charge, which correlates to the enhanced flatband shift and the increase in effective oxide charge, when higher voltage and longer stress times are applied. The J-E characteristics for both samples were compared and it was found that for the phosphorus doped SiO_2 samples, the breakdown electric field increased when the same measurements are repeated. The same mechanism of electron trapping and electron injection into the oxide can be explained for the instability of phosphorus doped SiO_2 in 4H-SiC MOS capacitors.

Chapter 4

Influence of dielectric formation on the characteristics of 4H-SiC CMOS devices

4.1 Introduction

The ability of silicon carbide to switch at high frequencies, whilst being the most CMOS-compatible wide bandgap material opens up exciting opportunities for a wide range of digital and analogue based applications. In an effort to fully exploit the material properties of SiC for the realization of CMOS devices, a thorough understanding of the influence of the dielectric gate on device performance is imperative. Although a range of extraction methods have been developed to acquire the density of interface states [151], a number of research groups have demonstrated that the most accurate method to estimate the density of interface states uses the C-ψ technique, derived from quasi-static capacitance-voltage (C-V) measurements [121]. Reports in the literature have demonstrated the investigation of $D_{\rm it}$ utilising C-ψ based on nMOS devices [67, 68, 121]. However, no comprehensive investigations have been performed on the pMOS counterpart nor the technique used to evaluate the oxide quality of complementary MOS. It is well known that the interface properties of Si/SiO_2 layers defines the electrical performance of a MOS devices, therefore it is critical to accurately determine $D_{\rm it}$ [193]. Furthermore, the low channel mobility commonly observed in SiC MOSFETs is linked to the high density of interface states, where such limitation hinders the uptake of silicon carbide technology in integrated circuits [19]. Intensive research varying the annealing of dielectric films including the use of hydrogen [66], nitrogen [194] and phosphorus [2] has been undertaken in an attempt to passivate the interface traps. This has led to the increase of field effect mobility up to 284 cm^2/Vs at room temperature for MOSFETs fabricated with an ultrathin thermally grown SiO_2 inserted between the Al_2O_3 and SiC [102].

4.2 Experimental: Processing techniques for the formation of dielectric

In this investigation, 3 gate dielectrics on both n-type and p-type of MOS capacitors and MOSFETs that have undergone different process treatments were measured. All devices are nominally identical except for the gate dielectric formation. The objective of this investigation

is to distinguish each process treatment in term of the electrical characteristics. The details of dielectric formation are summarized in the Table 4.1. MOS capacitor and field effect transistor (MOSFET) structures were fabricated using a CMOS process [7] on commercial grade 100 mm, Si face, 4° off axis, 4H-SiC n-type substrate wafers. Figure 4.1 shows a schematic cross section of the fabricated a) lateral nMOS capacitor and b) p-channel MOSFET. A polycrystalline silicon layer (area =160,000 μm^2) was deposited on the deposited gate dielectric, while Al based metal contacts were patterned to form the lateral capacitor electrode and the drain/source contact for the MOSFET. The fabricated p-channel MOSFET exhibits a gate geometry of 200 μm $\times$1.2 μm. Conversely, equivalent pMOS variants were fabricated on a p type epitaxy. These devices were fabricated on epitaxial layers doped with nitrogen (N_{D}=1.50 $\times 10^{17}$ cm^{-3}) and aluminium (N_{A}=1.02$\times 10^{17}$ cm^{-3}) for the nMOS and pMOS devices respectively. No threshold adjustment implants were used in the fabrication process, hence the electrical characteristics of the lateral capacitor and MOSFET are determined by the intrinsic properties of the SiO_2/SiC interface. The C-V, quasi-static C-V and current-voltage (I-V) measurements were performed using a Keithley 4200-SCS Parameter Analyser in conjunction with a Cascade Microtech probing station (Model Summit 12000BAP) supported on an active air anti-vibration table at room temperature under dark conditions.

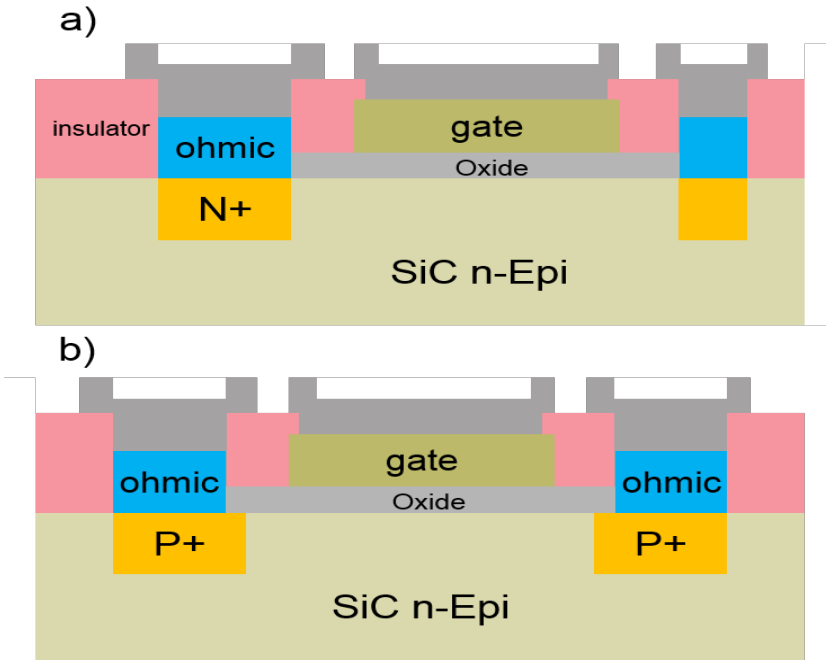


Figure 4.1: Schematic cross section of the SiC a) n-MOS capacitors and b) p-channel MOSFET on n-epilayer.

Table 4.1: Description of the processing steps used in the fabricarion of the dielectrics in sample A, B and C.

Samples	Description
A	High temperature post gate anneal (40 nm of SiO_2 by PECVD, 5 minutes dwell time at 1350°C)
B	Enhanced standard gate process (40 nm of SiO_2 by PECVD, N_2O + O_2 anneal at 800°C for 30 minutes)
C	Combination of sample A and B process (40 nm of SiO_2 by PECVD, 5 minutes dwell time at 1350°C, N_2O + O_2 anneal at 800°C)

4.3 SiO_2/SiC interface and impact of process variation

The electrical characteristics of both n-type and p-type 4H-SiC MOS capacitors such as interface state density, flatband voltage, threshold voltage and effective charge were extracted from C-V characteristics at room temperature. In addition, Fowler Nordheim plots extracted from the current density-voltage data are also analysed to understand the leakage mechanism and provide new insights into the reliability and breakdown issue in SiC MOS capacitors.

4.3.1 Impact of the dielectric formation on the characteristics of n-type MOS capacitor

The data in Figures 4.2 (a) and (b) show the variation of 1 MHz capacitance as a function of voltage and the variation of normalised capacitance as a function of voltage for samples A, B and C respectively. The oxide capacitance in the accumulation region of each sample are different because of the variations in oxide thickness. Sample C exhibits the lowest oxide capacitance value due to the long oxidation process that produces thicker gate dielectric in comparison to the other samples.

Table 4.2: Summary of parameters extracted from n-type MOS capacitors.

Samples	Effective oxide thickness (nm)	Flatband votage (V)	Threshold voltage (V)	Effective oxide charge (C/cm^{-2})
A	37.7	1.7	-5.2	-8.2×10^{11}
B	41.7	1.7	-5.56	-7.4×10^{11}
C	42.8	0.35	-6.9	-0.4×10^{11}

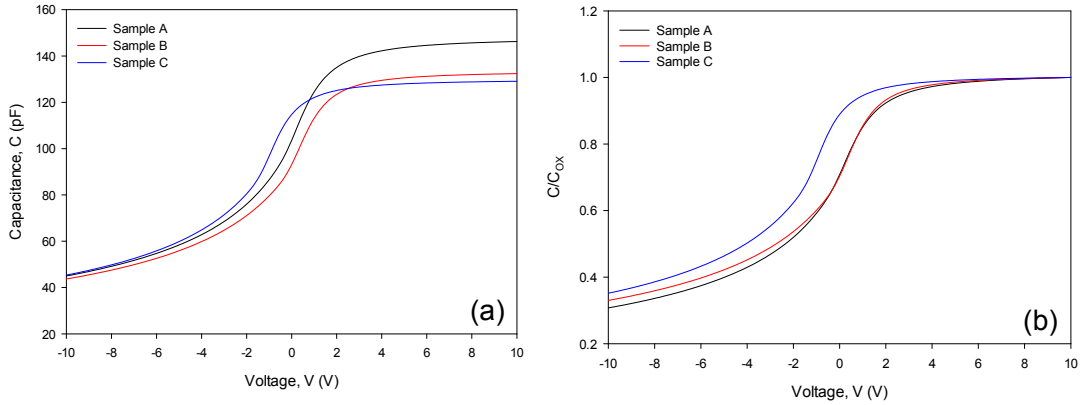


Figure 4.2: (a) 1 MHz Capacitance-Voltage characteristics (b) Normalised 1 MHz Capacitance-Voltage characteristics for n-type MOS capacitor with different dielectric formation (Sample A, B and C).

The data in Table 4.2 show the extracted parameters for each n-type MOS capacitors samples A, B and C. The effective oxide thickness, T_{OX}, was extracted using a relative permittivity, ε_r of 3.9 for SiO_2. V_{FB} defines the boundary of the capacitor accumulation and depletion regions, whilst V_{TH} demarcates the depletion and inversion regimes. From the data, values of V_{FB} can be determined, which are 1.7 V, 1.7 V and 0.35 V for samples A, B and C respectively. The variation in V_{FB} results in a reduction in the threshold voltage of the MOSFET. Typically, V_{FB} for an ideal SiO_2/SiC interface that has zero N_{EFF}, is defined by the metal-semiconductor work function difference. The work function is derived as

$$W_{MS} = W_M - \left[W_{SiC} + \left(\frac{E_G}{2}\right) - \Phi_B\right] \tag{4.1}$$

where, W_{MS} is the metal–semiconductor work function, W_S the metal work function, W_{SiC} the SiC work function, E_G is the bandgap of SiC and Φ_B is the bulk potential. It is clear that the magnitude of V_{FB} for sample C is significantly smaller than that in samples A or B, indicating a smaller density of oxide charge in the nMOS capacitor structure and this can be described using effective charge density (N_{EFF}) [32].

It is well known that the magnitude of the extracted N_{EFF} comprises contributions from oxide trapped charge, fixed oxide charge, mobile charge and interface charge trapped by slow traps [150, 195, 196], where the total charge trapped in interface states are described by D_{it}. The data in Figure 4.3 show the extracted values of D_{it} using the C-ψ technique for n-type MOS capacitors between 0.2 and 0.5 eV from the conduction band edge, extracted from room temperature quasi-static C-V measurements [121]. As can be seen from the data, the value of

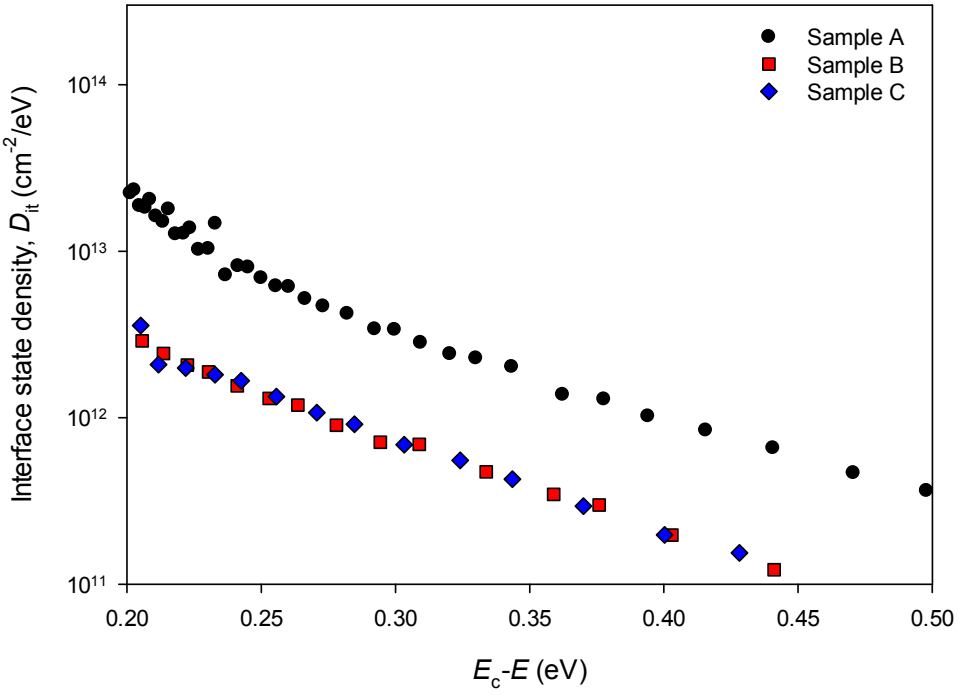


Figure 4.3: Interface state density as a function of energy extracted by C-ψ technique for n-type MOS capacitors.

$D_{\rm it}$ at $E_C - E = 0.2$ eV for sample A is approximately 2×10^{13} cm^{-2} eV^{-1}, which is one order of magnitude higher than samples B or C, which are approximately 2×10^{12} cm^{-2} eV^{-1} (these values are relatively large in comparison to silicon devices which is around 10^{10} cm^{-2} eV^{-1}). The value of $D_{\rm it}$ for sample A is always one order of magnitude higher in comparison to samples B and C for the range of energies considered here. The $D_{\rm it}$ values for both samples B and C are very similar to each other, which suggests that the traps at this energy level have been passivated for these two samples by nitrogen during the post-oxide -annealing in N_2O + O_2 [54, 57, 173]. The process of high temperature annealing at 1350°C during formation of gate dielectric in sample A however could not passivate the traps at the interface, resulting in the observed high interface state density along the energy band. The high temperature annealing might also increase the surface roughness at SiO_2/SiC.

I-V measurements were performed to examine the conduction mechanisms in each of the MOS capacitor samples. Different sizes of capacitors were measured to check the current uniformity. The data in Figure 4.4 show the current density as a function of electric field (J-E) characteristics of typical n-type MOS capacitors for each of the sample under positive gate biases (accumulation region). A non-destructive breakdown voltage is defined as the

field that results in a current density level of 1mA cm^{-2}, whilst a catastrophic breakdown indicates destructive oxide tunnelling. The J-E plots (Fig 4.4) show that sample B and C display a dielectric breakdown field at about 9.5 MV/cm followed by sample A at about 11.8 MV/cm [197]. These values are similar to dielectric breakdown field of SiO_2 on silicon which is typically above 9 MV/cm [198, 199].

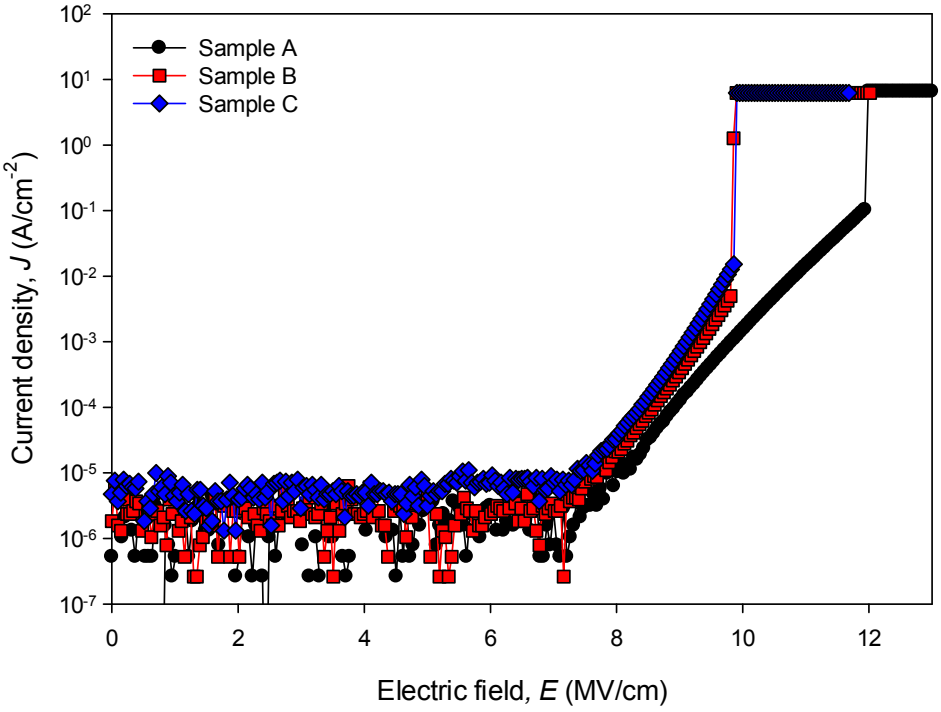


Figure 4.4: Current density- Electric Field, J-E for n-type MOS capacitors with different dielectric formation in accumulation. The area of MOS capacitors are 1.35×10^{-3} cm^2.

In general, the tunneling is elastic at higher electric fields and inelastic at lower fields. Hence, the influence of lower field on the current is not strong enough and thus noise level dominates current [192]. At high electrical fields Fowler Nordheim analysis allowed the barrier heights formed at defects in the oxide of 2.4 to 2.5 eV to be determined for all n-type capacitors (using the electron mass in oxide, m_{ox} of 0.42 m_e [180, 192, 200]) as shown in Figure 4.5. The effective barrier height may change due to variations in the defects at the SiO_2/SiC interface and oxide properties and depends on the conditions during oxide formation.

The intercept of this linear $\ln(J/E^2)$ as a function of $1/E_{\mathrm{OX}}$ gives A and the slope yields B [180]. As can be seen in the F-N plots (Figure 4.5), the linear trend at high electric field (above approximately 8 MV/cm) indicates the occurrence of FN tunnelling mechanism. The variation in the fabrication process of the gate dielectrics in this work results in a significant

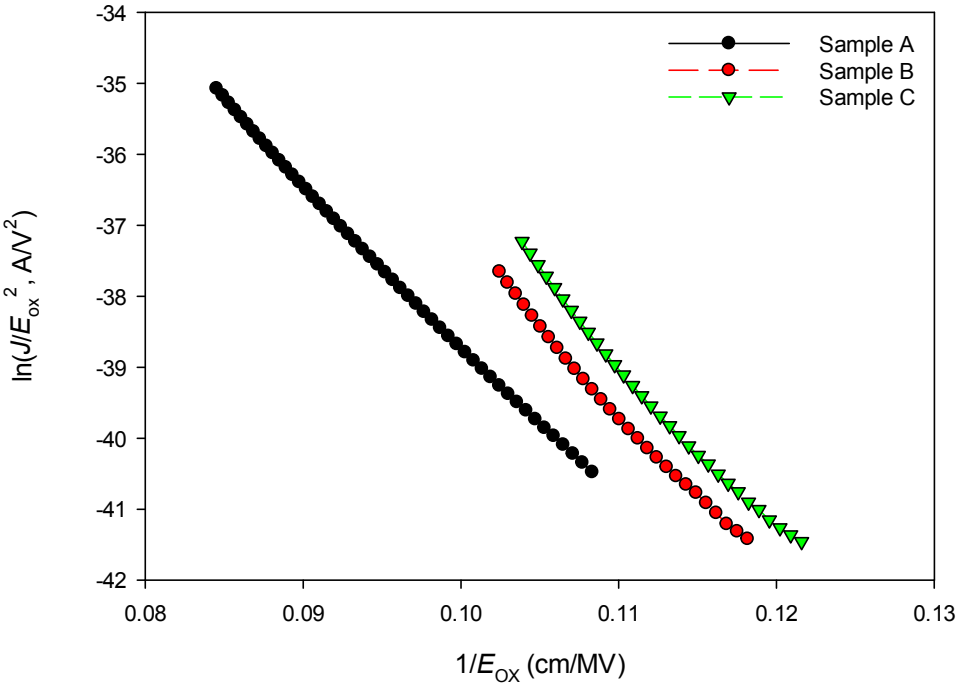


Figure 4.5: FN-plots for n-type MOS capacitors obtained from current-voltage measurements. From the slope, barrier heights of 2.4 to 2.5 eV were extracted. These values are close to the theoretical value of 2.7 eV [181, 183, 192].

difference in the effective barrier height for each of the samples. As can be observed from the similarity of the slope, sample C shows the onset of F-N tunnelling mechanism at a lower electric field, at $1/E_{\mathrm{OX}}$ of 0.12 cm/MV (E_{OX}=8.3 MV/cm), then followed by sample B at 0.11 cm/MV (E_{OX}=9 MV/cm) and sample A at 0.10 cm/MV (E_{OX}=10 MV/cm). The electron conduction through the oxide occurs in sample C at a lower electric field in comparison to the other samples and this maybe correlated with the observed lower breakdown voltage. The degradation of dielectric breakdown field in samples B and C could be related to the presence of nitrogen such as Si-N bonds at the SiO_2/SiC interface and in the SiO_2 bulk oxide [201, 202]. This suggests that high temperature annealing in the fabrication process for sample A results in high breakdown voltage. All the MOS capacitors sustain electric fields exceeding 9.5 MV/cm before breakdown, which is in good agreement with the results of SiO_2 breakdown field in the literature [2, 98, 200]. FN tunneling currents are expected to be much higher for a SiC-MOS capacitors than for a Si-based device for the same electric field because the conduction band offset between SiC and SiO_2 is smaller (2.7 eV) than that between Si and SiO_2 (3.2 eV). Due to that reason, the reliability of conventional SiC NMOS device is expected to be lower than Si NMOS devices under typical operating conditions. It has been reported that the location and

density of interface states within the bandgap influences not only channel mobility, but also the FN tunneling currents at the SiC-dielectric interface [203]. However, the results obtained in this work show no correlation between interface state density and oxide breakdown.

4.3.2 Impact of the dielectric formation on the characteristics of p-type MOS capacitor

The data in Figure 4.6 (a) and (b) show the room temperature 1 MHz C-V characteristics and normalised 1 MHz C-V characteristics for p-type MOS capacitors on samples A, B and C respectively. As mentioned previously for n-type MOS capacitors, the variation in the oxide capacitance in the accumulation region is due to variation in thickness arising from the gate dielectric process (Figure 4.6 (b)). Sample C exhibits the lowest oxide capacitance value, due to the longer oxidation process that results in a thicker gate dielectric in comparison to the other samples.

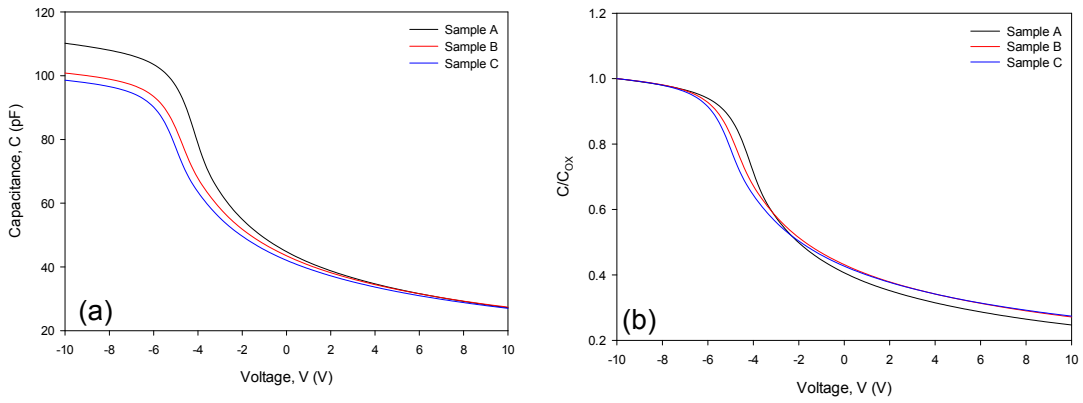


Figure 4.6: (a) 1 MHz Capacitance-Voltage characteristics (b) Normalised 1 MHz Capacitance-Voltage characteristics for p-type MOS capacitor with different dielectric formation (Sample A, B and C)

Table 4.3: Summary of parameters extracted from p-type MOS capacitors.

Samples	Effective oxide thickness (nm)	Flatband votage (V)	Threshold voltage (V)	Effective oxide charge (C/cm^{-2})
A	38.2	-5.05	1.10	1.31×10^{12}
B	42.3	-5.55	0.94	1.44×10^{12}
C	43.6	-5.8	0.8	1.52×10^{12}

Table 4.3 summarises the important parameters extracted from C-V measurements including oxide thickness, flatband voltage, threshold voltage and effective charge density for p-type MOS capacitors. The flatband voltage indicates the presence of charge in the oxide [204, 205], and its variation results in a shift of the threshold voltage in the MOSFET. The charge trapped in the bulk of the dielectric can also be described using effective charge density [150, 195, 196]. Contrary to n-type MOS capacitors where sample C shows a low V_{FB} (0.35 V) and N_{EFF} (-0.4×10^{11} cm^{-2}), for the p-type MOS capacitors, sample A exhibits the lowest V_{FB} (-5.05 V) and N_{EFF} (1.31×10^{12} cm^{-2}). From these results, it is revealed that a combination of high temperature annealing and the enhanced standard gate process reduces the density of negative charges in the oxide for n-type MOS capacitors whilst the high temperature annealing (HTA) process reduces the density of positive charge in the oxide for p-type MOS capacitors.

The data in Figure 4.7 show the variation in D_{it} extracted for p-type samples using the C-ψ technique from room temperature quasi-static C-V measurements [121]. The voltage was swept from accumulation to depletion at a rate of 0.1V/s. The data show the variation of D_{it} with energy near the valence band. It can be seen that sample A has a higher interface state density for energies between 0.2 and 0.5 eV in comparison to samples A and B. The same

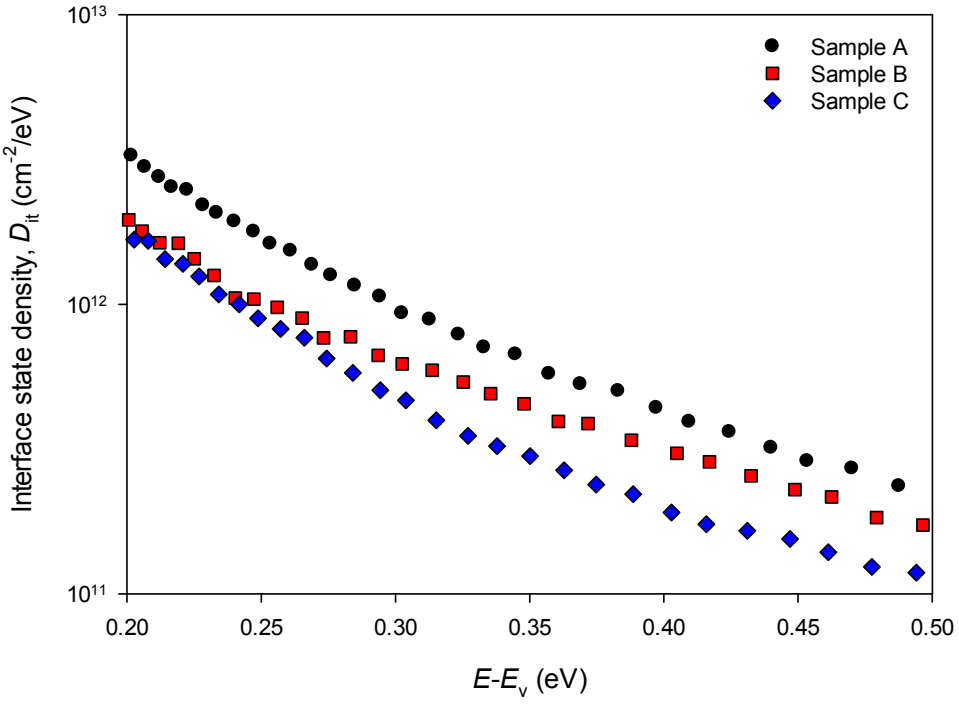


Figure 4.7: Interface state density as a function of energy extracted by C-ψ method for p-type MOS capacitors.

trend of $D_{\rm it}$ reduction can be observed but the values of $D_{\rm it}$ at $E - E_V$=0.2 eV for samples B and C are slightly lower than sample A being approximately equal at 2×10^{12} cm^{-2}eV^{-1}. However the interface state density for sample C reduces significantly at energies further from the valence band. The results show that high-temperature post gate anneal processes results in high $D_{\rm it}$ for p-type MOS capacitors, probably due to the formation of surface roughness at the SiO_2/SiC interface that is mainly responsible for the decrease in drain current at high gate drive bias (surface roughness scattering effect) [206–208]. However, the underlying mechanism has not been proven.

As with the n-type MOS capacitor samples, I-V measurements were performed on each of the p-type samples to understand the effect of dielectric formation on the current conduction mechanism in MOS structures. The data in Figure 4.8 show the leakage current density of each sample under negative gate bias at room temperature. At low electric fields, all samples show a low current density of approximately 1×10^{-5} A/cm^{-2}. The occurrence of electron tunnelling appears in Sample A for fields in excess of 6 MV/cm while samples B and C exhibit FN behaviour at electric fields above 8 MV/cm. Although the current density of sample A is higher in comparison to samples B and C, sample A has the highest breakdown electric field at

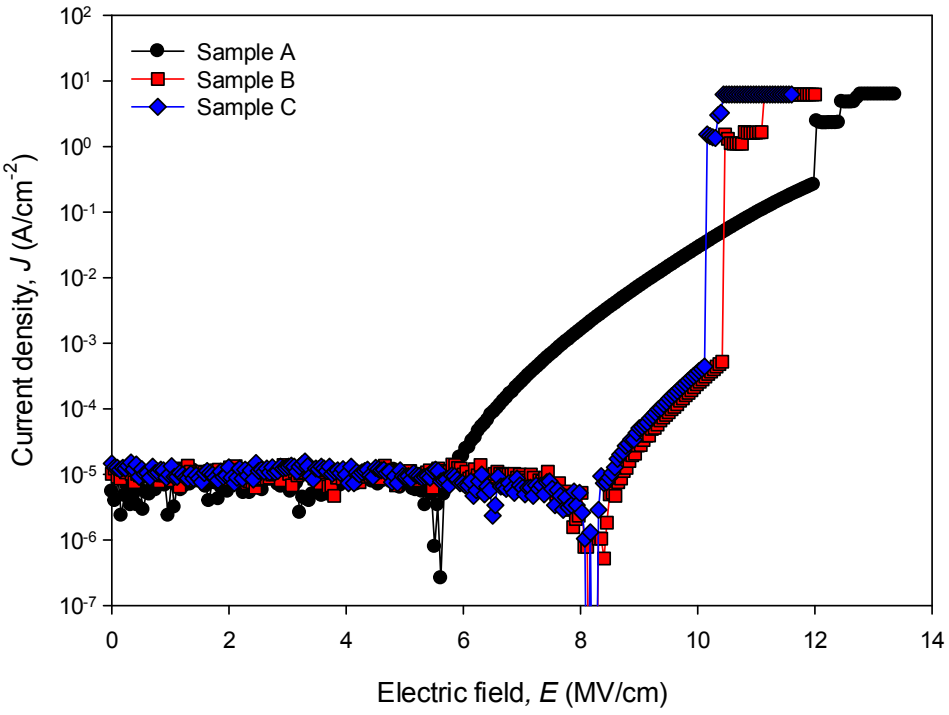


Figure 4.8: Current density- Electric Field, J-E for p-type MOS capacitors with different dielectric formation in accumulation. The area of MOS capacitors are 1.35×10^{-3} cm^2.

11.8 MV/cm, whereas samples B and C breakdown at 10.4 and 10.2 MV/cm respectively. This result is in good agreement with those in the literature [77, 209] where increased breakdown voltages were obtained for dielectrics annealed at higher temperature.

The data in Figure 4.9 show the FN plots of the p-type MOS capacitors at room temperature. As was observed in the n-type MOS capacitor data, a linear trend indicates the presence of the FN tunneling mechanism at high electric fields. Using Equations 4.1 to 3.12, the barrier height of each sample can be extracted. The barrier height for sample A, sample B and sample C are 1.48, 2.18 and 2.13 eV respectively. The effective mass for holes in silicon carbide in the calculations is 0.35 m_e [180]. These values of barrier height are in the range of reported values in the literature, which are from 1.2 to 3.1 eV [181]. The extracted value for the barrier heights are slightly lower that the theoretical value which is approximately 2.9 eV depending on the metal used as gate contact [23, 180, 181].

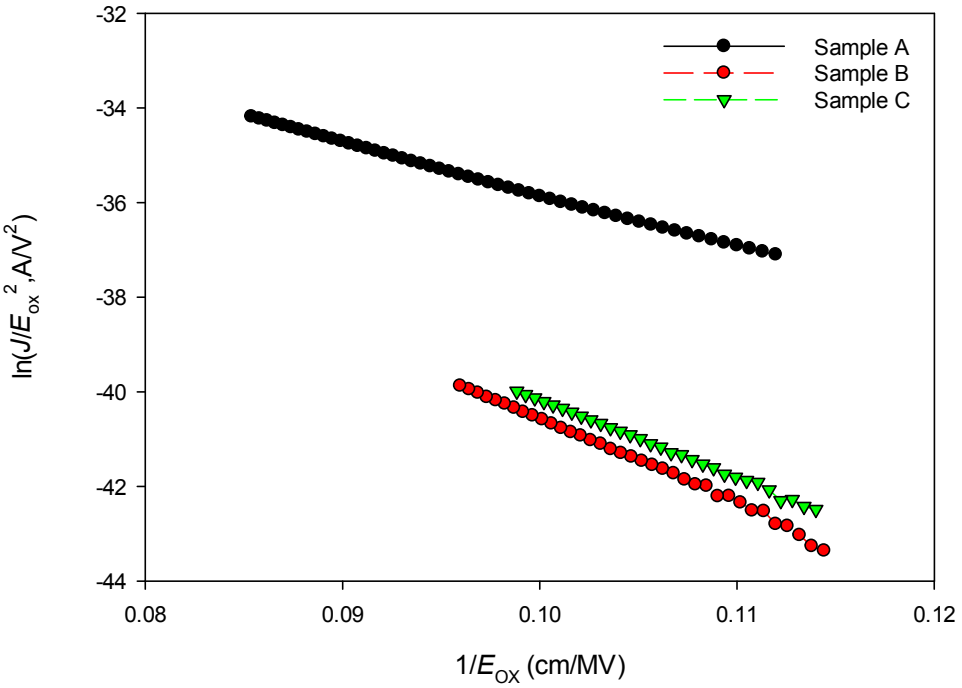


Figure 4.9: FN-plots for p-type MOS capacitors at room temperature. From the slope, a barrier heights of 1.48 to 2.18 eV are extracted. These values are quite far from the theoretical value of 2.9 eV.

4.4 Impact of elevated temperatures on MOS capacitors

In order to investigate the impact of gate dielectric formation on the electrical characteristics for both n and p-type MOS capacitors, 1 MHz C-V measurements were performed at temperatures from room temperature up to 400°C. The temperature dependence of important parameters including flatband voltage and interface state density were extracted and studied to determine the effect on the characteristics of the bulk oxide and the SiO_2/SiC interface.

4.4.1 Temperature dependence for n-type MOS capacitors

1 MHz C-V measurements were performed on samples A, B and C from room temperature to 400°C. The data in Figures 4.10 (a), (b) and (c) show the C-V characteristics of n-type MOS capacitors at elevated temperatures for samples A, B and C respectively. All samples exhibit stable C-V characteristics at elevated temperatures with a constant oxide capacitance and negligible shift in the C-V curves. This suggests that no physical change occurs in terms of the dielectric constant and oxide thickness with increasing temperatures.

To examine the effect of dielectric fabrication process on the stability of flatband voltage, the change in flatband voltage as a function of temperature was extracted and plotted as shown in Figure 4.11. The change in effective oxide charge, N_{EFF}, is also plotted in the same Figure. As can be seen from the data, sample C exhibits the smallest flatband voltage shift with only a 0.2 V shift observed between 25°C and 400°C. In contrast, the shift in flatband voltage for samples A and B are significantly larger with 0.5 and 0.8 V between 25° and 400°C. The data for effective oxide charge in the same figure show that sample C has a positive value, whilst samples A and B have negative effective oxide charges.

From the C-V data at elevated temperatures, the interface state density was extracted using the Terman method [118] as a function of energy. The experimental measurements required for the C-ψ technique, quasi static capacitance, can only be performed on samples with an extremely low leakage current. Quasi-static measurement is performed at a very low frequency (that is almost DC) with the ramp rate of 0.1V/s DC voltage and measuring the resulting current or charge. The leakage current of femtoamps or less can cause appreciable errors in the capacitance measurement (the current is no longer proportional to the capacitance). However, when the temperature of the measurement is increased, the leakage current through the oxide increases exponentially and so this measurement is no longer possible [191, 192, 210].

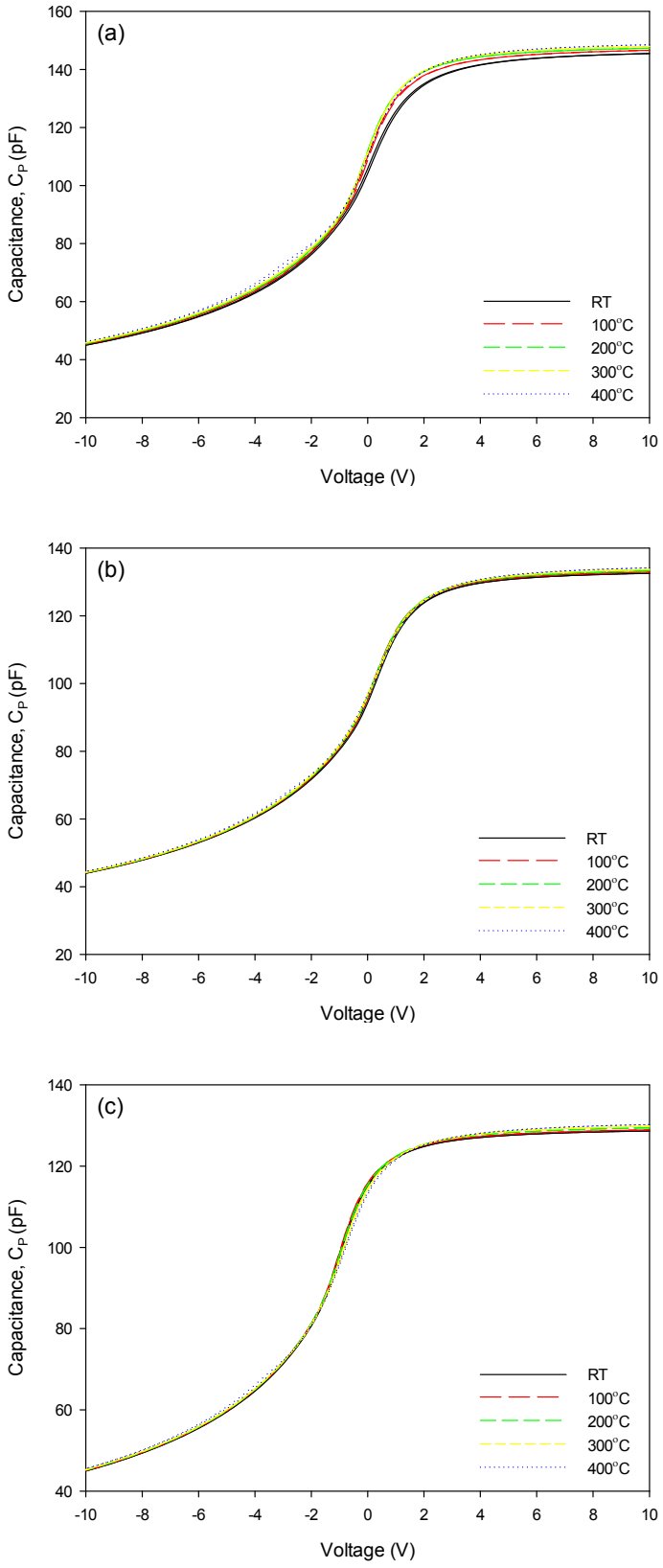


Figure 4.10: 1 MHz Capacitance-Voltage characteristics for Sample A (a), B (b) and C (c) n-type MOS capacitor from RT to 400°C.

In order to enable the temperature variation of D_{it} to be determined, the Terman technique was utilised because this is based on the measurement of a high frequency C-V curve, it is more

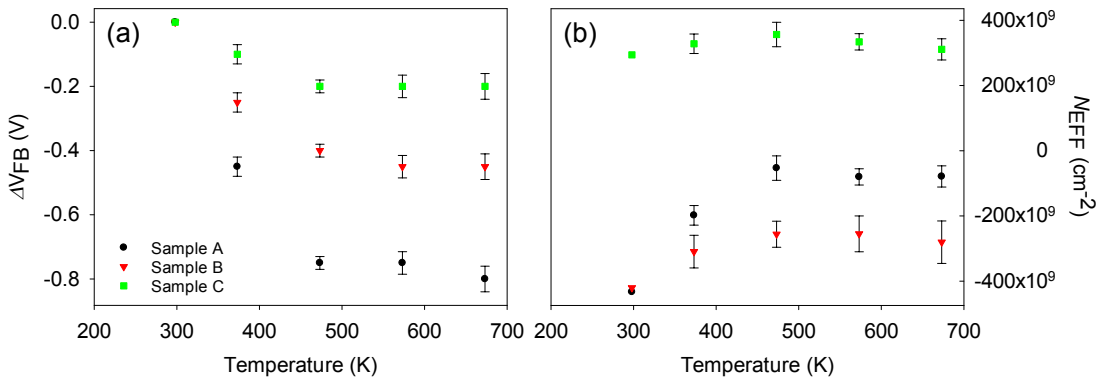


Figure 4.11: Variation of (a) V_{FB} and (b) N_{EFF} for all sample n-type MOS capacitor from RT to 400°C.

easily measured at high temperatures. The other advantage of the Terman technique is that it allows a direct comparison to other data that has been published in the literature. The data in Figure 4.12 show the interface state density as a function of temperature for n-type MOS capacitor samples A, B and C. The data show that the detected interface state density reduces with increasing temperature across the measured energy range for the three n-type samples studied here. This indicates that the interface state density has a temperature dependence and contains electrically active trapping states at elevated temperature. The data show that the interface state density near the conduction band reduces with elevated temperature as observed in previous work [99, 193] suggesting that the dominant scattering mechanism is Coulomb scattering.

This finding can also be explained by the bandgap narrowing effect as the temperature increases [119, 123, 182, 191, 211]. As shown by the data in Figure 4.13, the Fermi level becomes closer to the mid bandgap at elevated temperature. Therefore, the number of filled interface traps are fewer because the Fermi level is moving away from the band edge where D_{it} is high. The mobility of a MOSFET is expected to increase with temperature as a direct result of lower interface traps detected at the interface, hence reducing the Coulomb scattering. This result can also be explained by thermally activated transport or electron localization in the inversion layer where at the high temperatures the carriers have sufficient energy to detrap, reducing the filled interface state density at elevated temperatures [11, 125, 165, 212]. This effect is also know as the "electron trapping effect". The interface state density is high ($\sim 1\times10^{12}$ cm^{-2}eV^{-1}) which is comparable to the electron density at the SiO_2/SiC interface at room temperature. The trapped electrons are immobile but at elevated temperatures, more electrons are de-trapped and become mobile with increasing temperature. This is in good

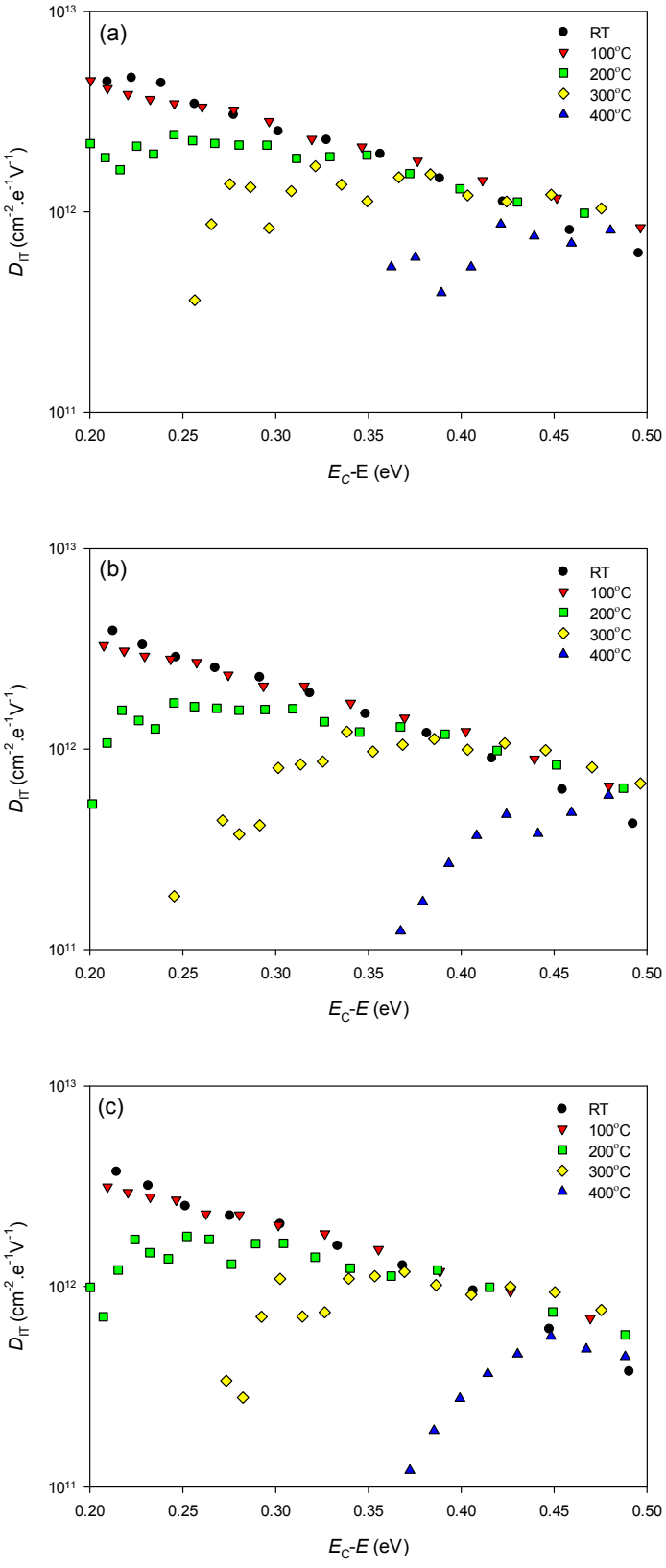


Figure 4.12: Interface state density as a function of energy for Sample A (a), B (b) and C (c) n-type MOS capacitor from RT to 400°C.

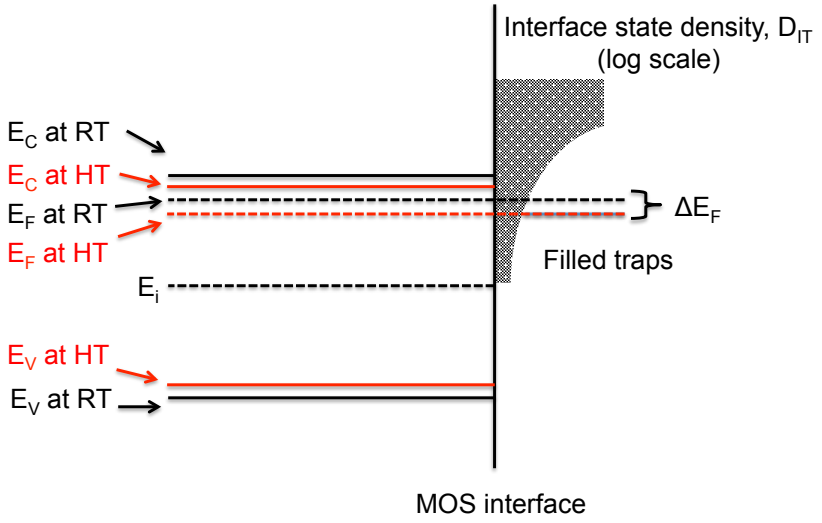


Figure 4.13: Illustration of bandgap narrowing effect from room temperature to high temperature. The position of Fermi level moves toward midgap with increase in temperature results in a reduction of interface state density.

agreement with the analytical modelling of thermally activated transport in SiC inversion layers [113, 193, 213].

4.4.2 Temperature dependence for p-type MOS capacitors

Similar to n-type MOS capacitors, 1 MHz C-V measurements were also performed on p-type MOS capacitors from room temperature to 400°C. The data in Figure 4.14 show the C-V characteristics of p-type MOS capacitors at elevated temperatures for samples A, B and C respectively. All samples exhibit stable C-V characteristics at elevated temperatures with similar oxide capacitance under accumulation. The shift in C-V curves with temperature is more prominent than that observed in the nMOS capacitors, especially for sample B.

As with the n-type MOS capacitors, the change in flatband voltage at elevated temperatures was extracted and plotted in Figure 4.15. The change in effective oxide charge, N_{EFF} was also plotted in the same Figure. As can be seen from the data, the change in flatband voltage for all samples is similar with the temperature. This shift in flatband voltage is due to the impact of the elevated temperature on the bandgap of the 4H-SiC and the change in the intrinsic carrier concentration [18]. The data for effective oxide charge in the same figure show that all the samples have positive values of effective oxide charge. As shown in equations 3.4 and 3.5, the effective oxide charge has a strong dependence on the change in flatband voltage. Due to that

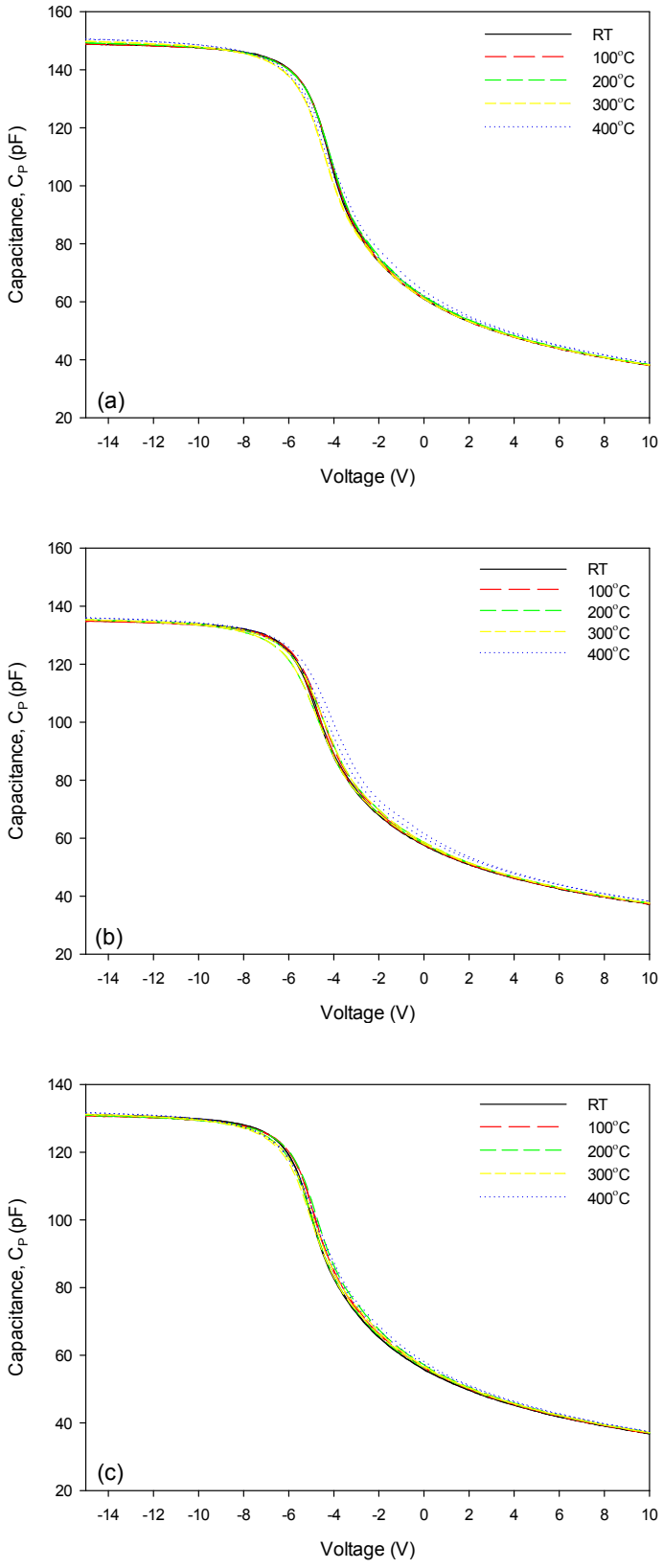


Figure 4.14: 1 MHz Capacitance-Voltage characteristics for Sample A (a), B (b) and C (c) p-type MOS capacitor from RT to 400°C.

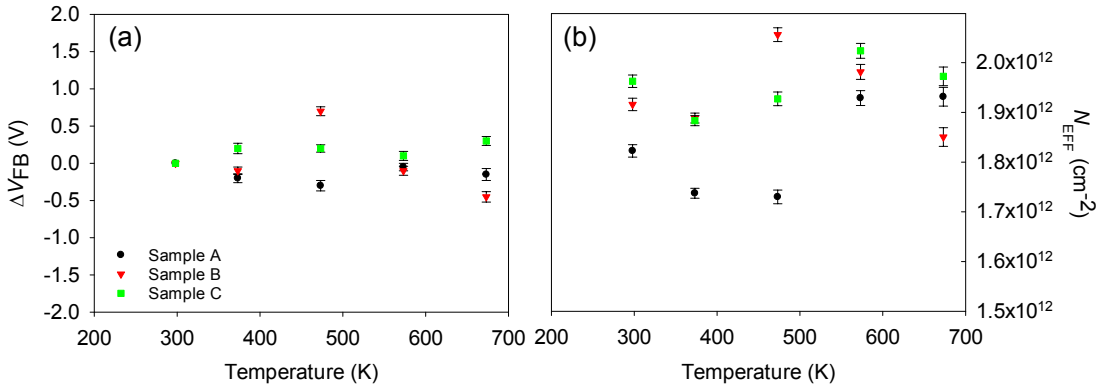


Figure 4.15: Variation of (a) V_{FB} and (b) N_{EFF} for all sample p-type MOS capacitor from RT to 400°C.

reason, the value of the effective oxide charge for samples A, B and C is also stable with the increasing temperature.

The interface state density as a function of energy within the bandgap was extracted from the measured C-V data using the Terman method. As can be seen from the data in Figure 4.16, all samples show the same trend, with a reduction in interface state density not only near the valence band but also across the energy range studied with increasing temperature. The data indicate that trapped carriers are released (detrapped) as the temperature is increased. As mentioned before in section 5.51, the decrease in interface state density with increasing temperature is due to the bandgap narrowing effect [151, 182]. These results are in good agreement with those published previously [123] where the increase in temperature does not have a significant effect on the midgap densities for both n and p-type MOS 4H-SiC due to the location of high density interface state that is close to the edge of conduction and valence band respectively.

4.5 Impact of dielectric formation and processing on SiC MOSFETs at RT

As was discussed in Chapter 2, SiC technology is significantly affected by the extremely low channel mobility and oxide reliability in comparison to silicon technology, due to issues at the SiC/SiO_2 interface. The channel mobility can be improved by the use of passivation techniques and using high-κ materials as the gate dielectric. Hence, there has been a significant amount of research in optimizing the formation of the gate dielectric. As described in the previous sections, the effect of different dielectric formation has been discussed based on the electrical

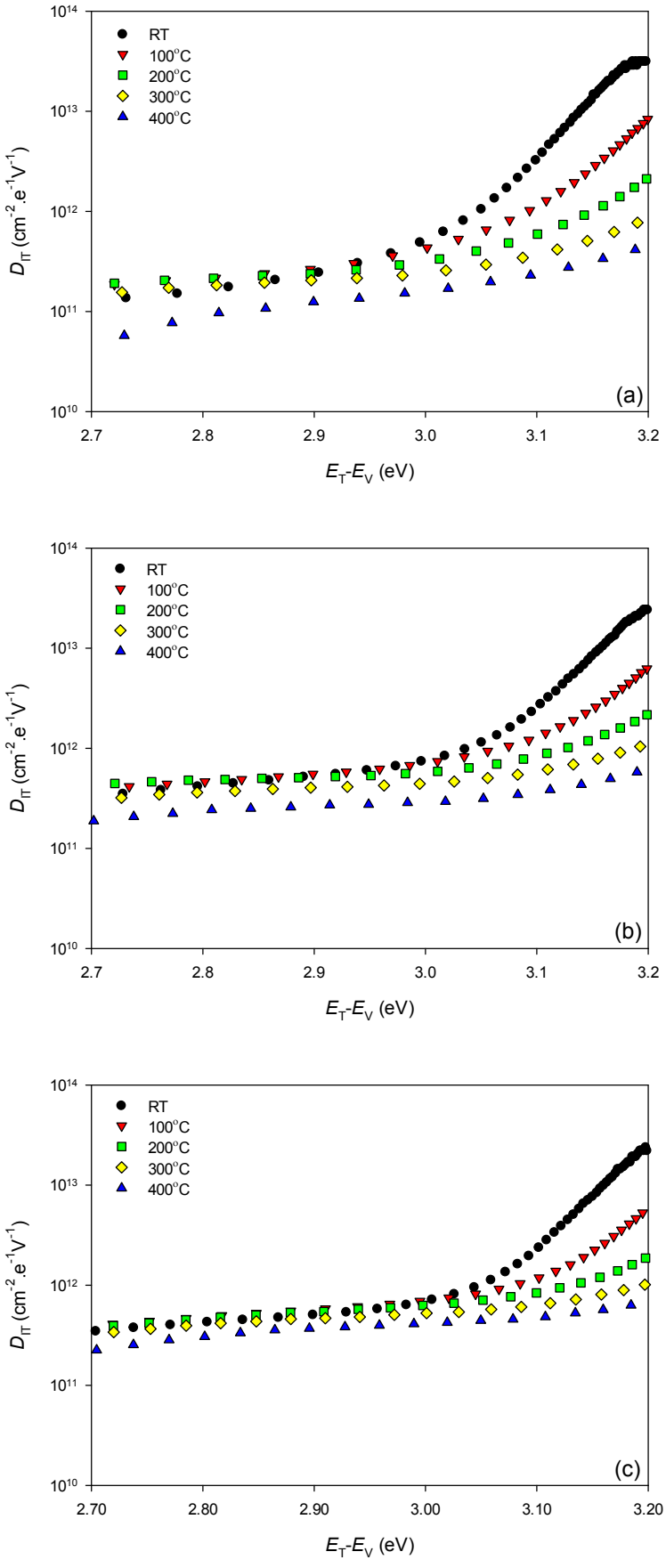


Figure 4.16: Interface state density as a function of energy for Sample A (a), B (b) and C (c) p-type MOS capacitor from RT to 400°C.

characteristics of MOS capacitors. In this section, the impact of dielectric formation will be determined from the electrical characteristics of MOSFETs.

4.5.1 Comparison for n-channel MOSFETs at room temperature

The data in Figure 4.17 show the field effect mobility as a function of gate overdrive (V_{G}-V_{TH}) for 1.2 μm $\times$ 200 μm n-channel transistors with different dielectric formation (samples A, B and C). The field effect mobility was extracted from the transconductance of current-voltage, (I_{D}-V_{G}) data at a drain bias of 0.1 V [151]. It can be noted that sample C has the highest peak field effect mobility, approximately 11 cm^2/Vs, followed by sample B with 10 cm^2/Vs and sample A at a 3 cm^2/Vs. The values of field effect mobility obtained for all three samples are low in comparison to a power device because the doping concentration of the p-epi layer is approximately 3 orders of magnitude higher than (N_{D}=1.50 $\times 10^{17}$ cm^{-3}). It is known that the electron mobility decreases with increasing dopant concentration in the bulk semiconductor due to the scattering at ionized acceptors [202]. The data for field effect mobility obtained in this experiment are in good agreement with those obtained for the interface state density from n-type MOS capacitors in Figure 4.3, where the field effect mobility is inversely proportional to the interface state density extracted using the C-ψ technique [111, 141].

4.5.2 Comparison for p-channel MOSFETs

As with n-channel MOSFETs, the data in Figure 4.18 show the field effect mobility as a function of gate overdrive (V_{G}-V_{TH}) for 1.2 μm $\times$ 200 μm p-channel transistors with different dielectric formation (samples A, B and C). The field effect mobility was extracted from the I-V, (I_{D}-V_{G}) data with drain bias of 0.1 V [151]. As can be seen from the data in Figure 4.18 , there are no significant differences in the peak field effect mobility, where all samples exhibit approximately, 4 cm^2/Vs. Since the data for field effect mobility obtained in this experiment are relatively low, no conclusive correlation can be given from the interface state density of p-type MOS capacitors in Figure 4.7.

As can be seen from the data in both Figures 4.17 and 4.18, Coulomb scattering dominates at low gate biases and the surface roughness scattering dominates at high gate biases. The results obtained follow the universal model for field effect mobility [113, 214, 215]. The peak mobility of the n-channel transistor is about 2 times higher than p-channel transistor due to the bulk

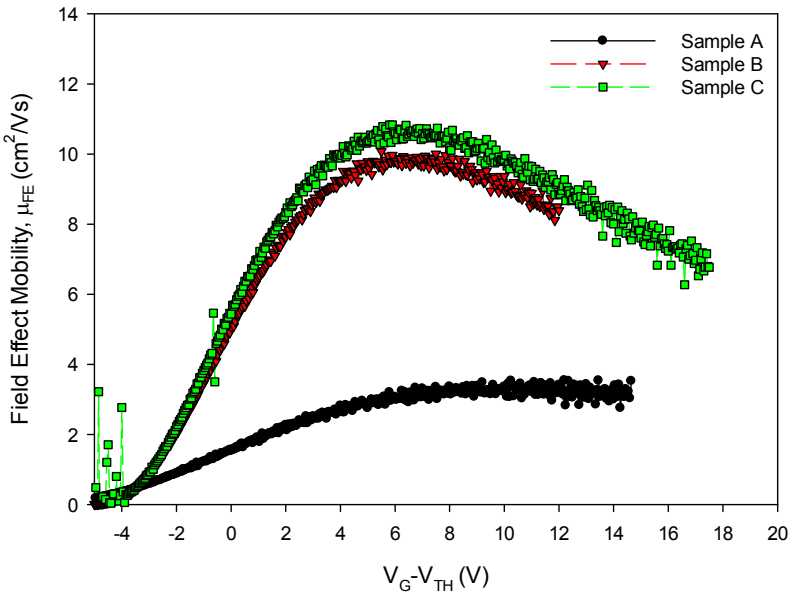


Figure 4.17: Comparison of field effect mobility as a function of voltage for n-channel samples A, B and C at room temperature. The size of transistor is L_G=1.2 μm, W_G=200 μm. The field effect mobility was extracted from data of I_D-V_G measured at room temperature with V_D=0.1 V.

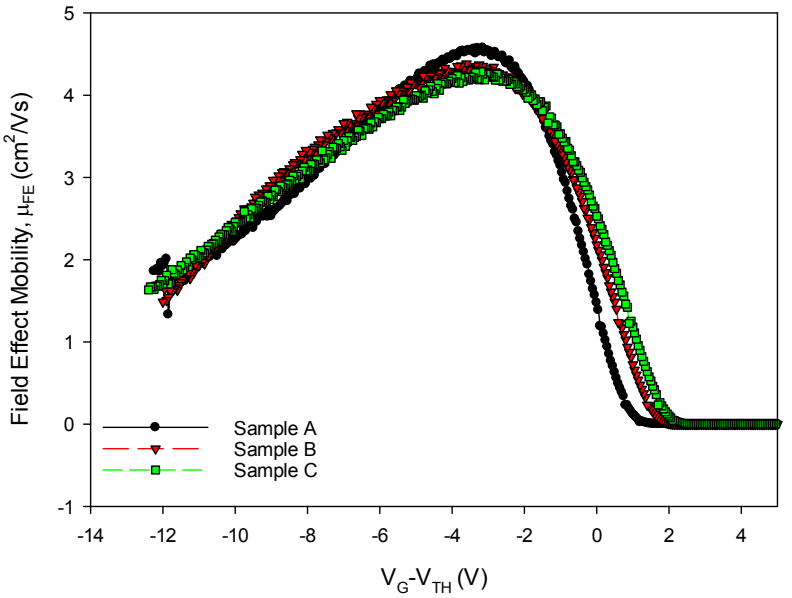


Figure 4.18: Comparison of field effect mobility as a function of voltage for p-channel samples A, B and C at room temperature. The size of transistor is L_G=1.2 μm, W_G=200 μm. The field effect mobility was extracted from data of I_D-V_G measured at room temperature with V_D=-0.1 V.

electron mobility being higher than the bulk hole mobility ($\mu_{\rm e}\simeq$600 cm^2/Vs, $\mu_{\rm h}\simeq$350 cm^2/Vs for dopant concentrations of 10^{17} cm^3). The mobility for n-channel and p-channel transistors are also correlated with the interface state density at the SiC/SiO_2 interface where the value of $D_{\rm it}$ near the band edges are 3×10^{12} cm^{-2} eV^{-1} and $2\times$ 10^{12} cm^{-2} eV^{-1} for both nMOS and pMOS respectively. The similarity in the observed voltage dependence for both nMOS and pMOS devices agrees with observations published elsewhere [216–219].

4.6 Impact of dielectric formation and processing on SiC MOSFETs at elevated temperatures

In this section, the impact of dielectric formation on SiC MOSFETs at elevated temperatures were investigated. This study involved the extraction of field effect mobility, threshold voltage and subthreshold swing (S) from the measured $I_{\rm D}$-$V_{\rm G}$ data from RT up to 400°C.

4.6.1 Temperature dependence for n-channel MOSFETs

The data in Figure 4.19 show the change in peak field effect mobility as a function of temperature for a 1.2 μm $\times$ 200 μm n-channel transistor with different dielectric formation (samples A, B and C). The peak of field effect mobility increases almost linearly for all samples up to 300°C as the trap occupancy reduces with temperature, thus reducing the effect of Coulomb scattering. However, the peak field effect mobility of samples B and C starts to saturate at 400°C with a value of approximately 16 cm^2/Vs. In general, the peak field effect mobility of sample C is always the highest across temperature range from RT to 400°C, followed by samples B and A. The increase in peak field effect mobility that can be observed in Figure 4.19 with increasing temperature is due to the decrease in interface state density near the conduction band. These results are in excellent agreement with the reported variation of the interface state density with temperature shown in Figures 4.16 (a), (b) and (c).

The change in threshold voltage with increasing temperature was also investigated. The data presented in Figure 4.20 show the change in the extracted threshold voltage with increasing temperature deduced from the linearly extrapolated value when the gate overdrive is zero. The data in the Figure show the difference in the threshold voltage for samples A, B and C. At room temperature, the threshold voltage for the samples was approximately 10, 8 and 7 V respectively. The threshold voltages reduced with increasing temperature and at temperatures

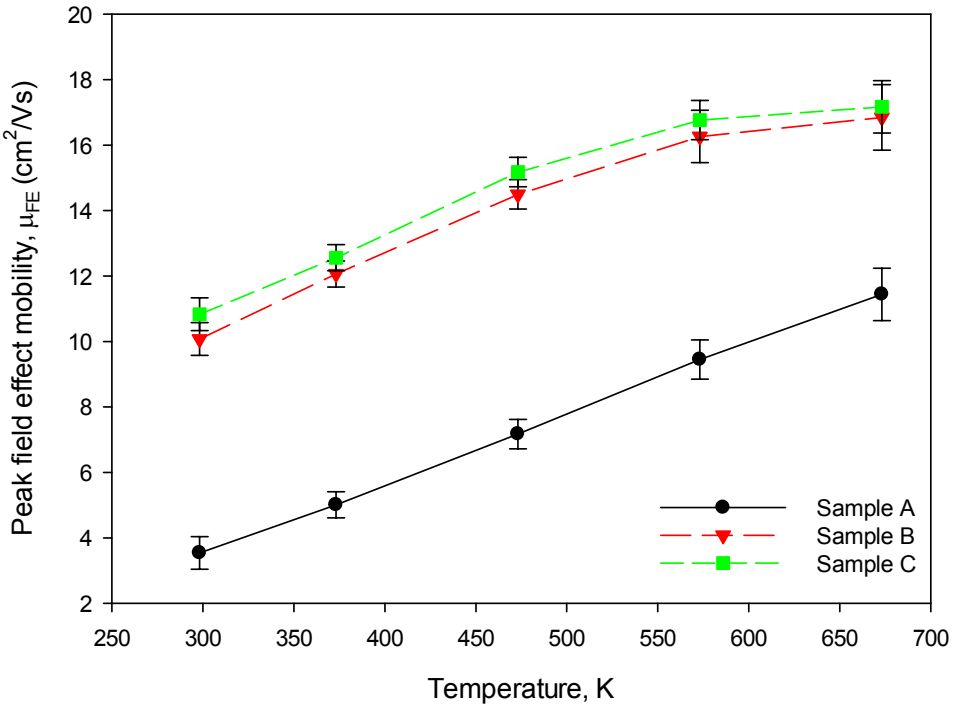


Figure 4.19: Change in peak field effect mobility of n-channel MOSFET for sample A, B and C from RT to 400°C.

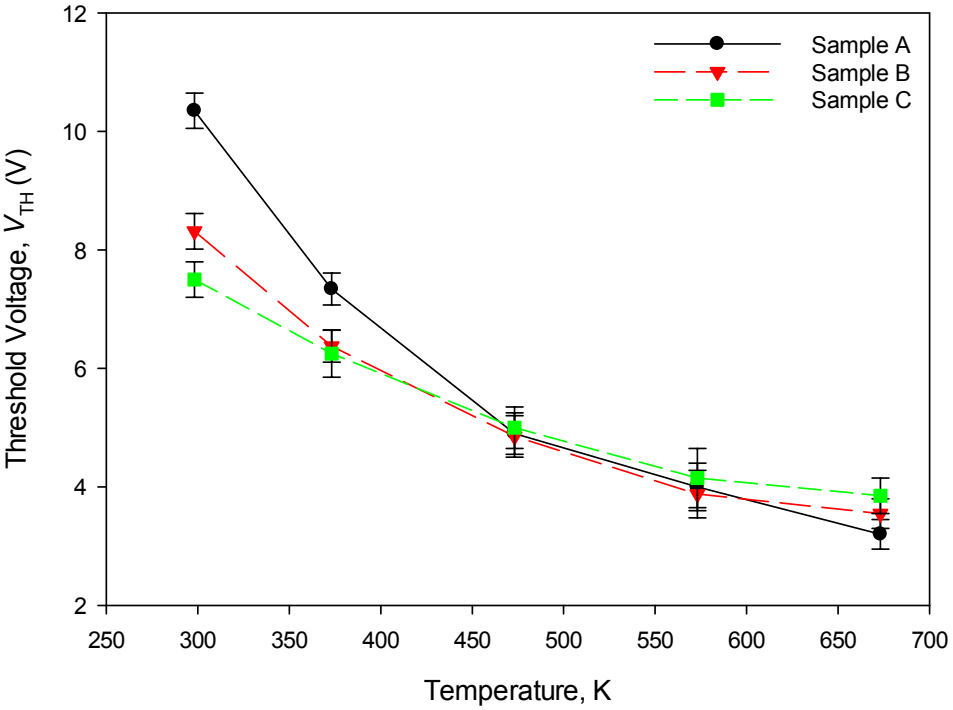


Figure 4.20: Change in threshold voltage, V_{TH} of n-channel MOSFET for sample A, B and C from RT to 400°C.

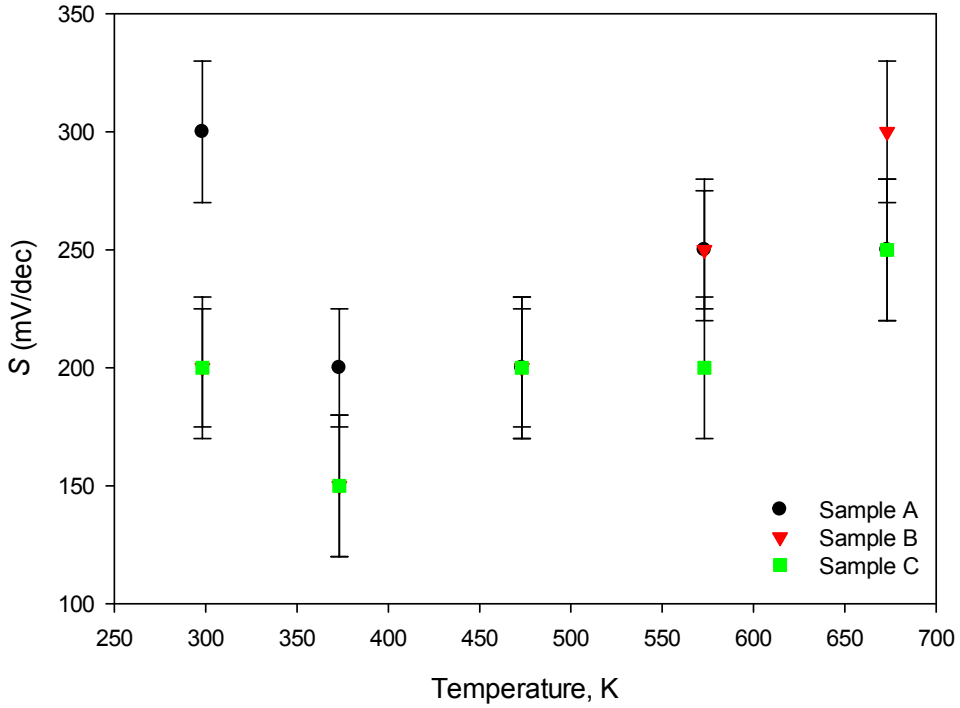


Figure 4.21: Substhrehold swing characteristics of n-channel MOSFET for sample A, B and C from RT to 400°C.

of 200°C and above, all samples exhibit a similar value of V_{TH}. The reduction of threshold voltage with increasing temperature occurs because the surface band bending required to form an inversion layer reduces as the temperature increases. This is also can be explained by the observed change in the density of the interface trap at the SiC/SiO_2 interface due to the bandgap narrowing effect or detrapping [156, 165, 182, 212].

The data in Figure 4.21 show the differences in subthreshold swing for samples A, B and C from room temperature up to 400°C. The subthreshold slope is expected to increase with temperature because S is proportional to kT/q as given in equation 2.42. Nevertheless, there is no significant trend observed in the subthreshold swing for all samples, however, the S for sample C is the most stable with a value in range of 150 to 250 mV/dec.

4.6.2 Temperature dependence for p-channel MOSFETs

The data in Figure 4.22 show the change in peak field effect mobility as a function of temperature for 1.2 μm $\times$ 200 μm p-channel transistor with different dielectrics. In contrast

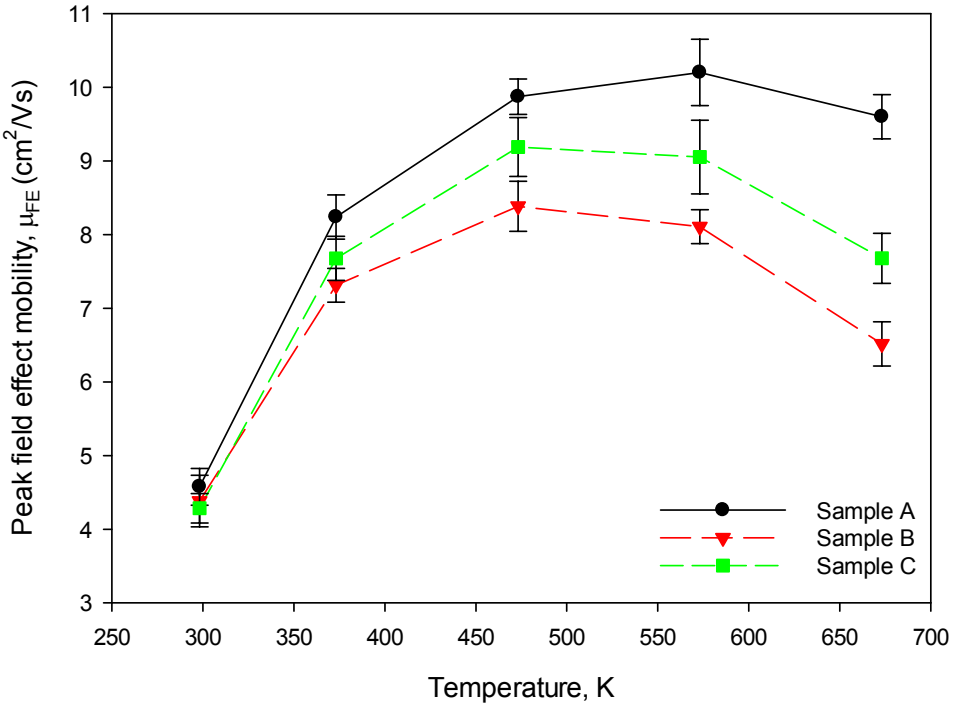


Figure 4.22: Change in peak field effect mobility of p-channel MOSFET for sample A, B and C from RT to 400°C.

to the data for field effect mobility in n-channel devices, the peak field effect mobility for p-channel MOSFETs increases gradually for all samples up to 200°C and then shows evidence of saturation with mobilities of approximately 10, 9 and 8 cm^2/Vs for samples A, C and B respectively. After 200°C, the peak field effect mobility for all samples decreases with further increases in temperature. The increase in peak field effect mobility shown in Figure 4.22 with temperature up to 200°C can be explained by the decrease in interface state density near the conduction band as shown in Figures 4.12. However, the reason for the reduction in the peak field effect mobility for temperatures above 300 °C still remains unclear. The results suggest that other mechanisms such as as phonon, bulk and surface roughness scattering are dominating the p-channel mobility approximately above this temperature. This result indicates that the temperature dependence of the mechanism at the SiC/SiO_2 interface for p-channel devices is not the same as for n-channel devices.

The change in threshold voltage with increasing temperature for p-channel MOSFETs was also investigated. The data presented in Figure 4.23 show the change in the extracted threshold voltage with the increasing temperature. The data in Figure 4.23 show the difference in threshold voltage for samples A, B and C at temperatures up to 400°C. At room temperature,

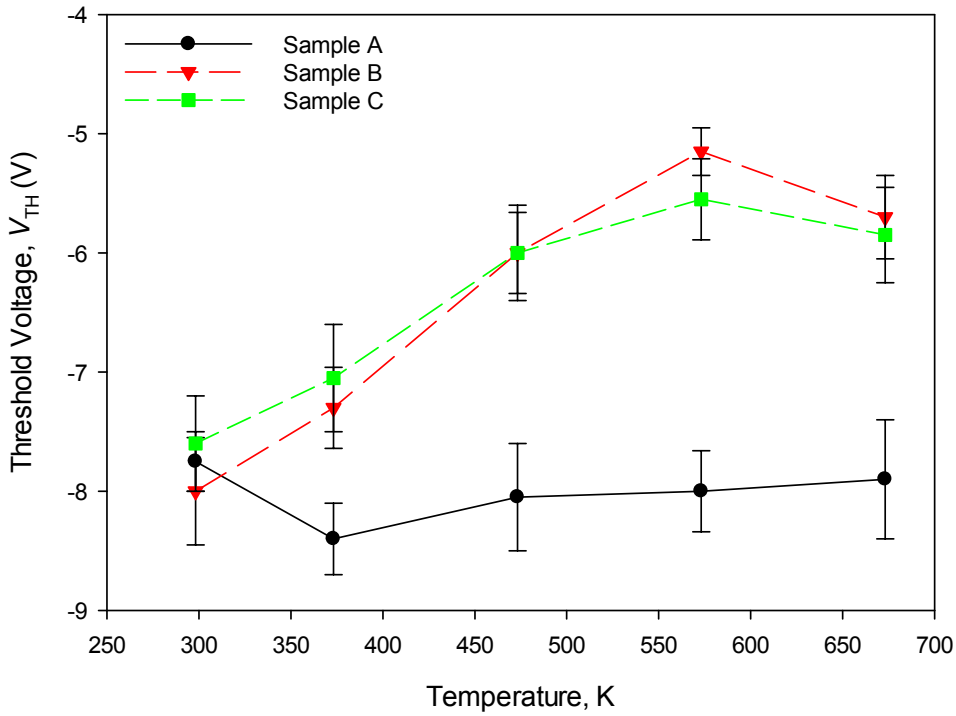


Figure 4.23: Change in threshold voltage, V_{TH} of p-channel MOSFET for sample A, B and C from RT to 400°C.

the threshold voltage for samples A, B and C was approximately -8 V. The threshold voltages for samples B and C reduce with increasing temperature and at 300°C and above, both samples exhibit similar value of V_{TH}. Similar to the behaviour observed in n-channel MOSFETs, the reduction of threshold voltage with increasing temperatures occurs in all samples because the required surface band bending for inversion reduces as the temperature increases. This is also can be explained by the change in the density of interface trap at SiC/SiO_2 due to the bandgap narrowing effect or carrier detrapping. In contrast, the threshold voltage for sample A remains almost constant at -8 V for the temperature range studied here. This indicates that no physical or chemical changes occur at the SiC/SiO_2 interface or in the bulk oxide for sample A. From these results, the formation of gate dielectric for sample A has shown good mobility characteristics and threshold voltage stability for temperatures up to 400°C.

The data in Figure 4.24 show the change in the subthreshold swing as a function of temperature for samples A, B and C for temperatures up to 400°C. Although sample A has shown good electrical characteristics in terms of mobility and V_{TH}, the S values are 2 times higher than for samples B and C.

In general, the total drain current for all n and p-channel samples increases with increasing

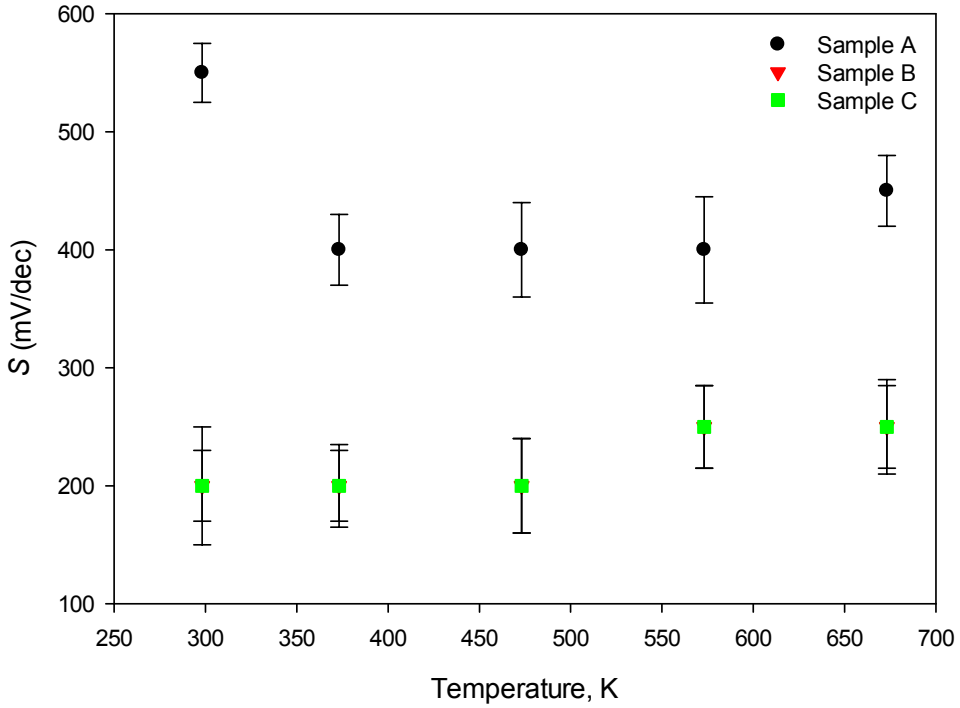


Figure 4.24: Subthrehold swing characteristics of p-channel MOSFET for sample A, B and C from RT to 400°C.

temperature between 25 and 300°C. There are a number of factors that cause the total drain current to increase. One of the main factors is the occupancy of traps at the SiC/SiO_2 interface. The reduction of trap occupancy at elevated temperature has increased the concentration of free carriers at the interface, resulting in an enhanced current flow and thus increase the field effect mobility. These results are in good agreement with the previously published physical model of high temperature operation of 4H-SiC that incorporates the influence of parameters including Coulomb scattering, phonon scattering, surface roughness scattering and interface state densities [220–222].

4.7 Inversion MOS capacitor

MOS capacitors have been used to study the quality and reliability of the 4H-SiC/SiO_2 interface. As a consequence of the large bandgap, the intrinsic carrier concentration and hence thermal generation of minority carriers in the 4H-SiC capacitor is low (5×10^{-9} cm^{-3} at the room temperature, which is relatively low in comparison to silicon 10^{10} cm^{-3}). Consequently, at room temperature MOS capacitors cannot reach thermal equilibrium and the C-V response

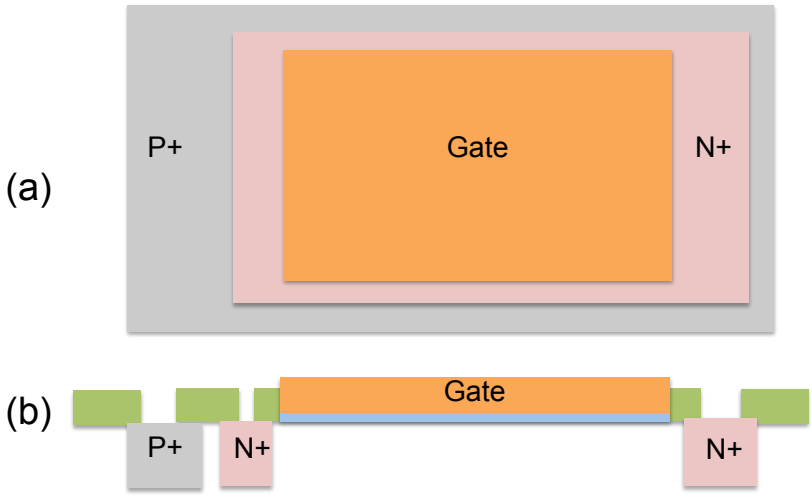


Figure 4.25: Schematic of p-type inversion MOS capacitor SiC from the (a) top view (b) cross section.

always shows a deep-depletion characteristic when measured in the dark. In addition, the surface states residing deep in the bandgap are not in equilibrium during the dc bias sweep and therefore go undetected during the measurement [223]. There are three mechanisms to speed up the generation of carriers in MOS capacitors; (1) optical generation (2) impact ionization (3) generation through defects. When the measurement is performed in the dark, the optical generation and impact ionization term are negligible for typical doping densities. Thus, the generation lifetimes is only due to defects in the semiconductor.

In this work, an n^+ (for p-type)/ p^+ (for n-type) implanted ring surrounds the MOS structure and is used as an external source of inversion charge to allow the measurement of deep level surface states at room temperature. Figures 4.25 (a) and (b) show the schematic of a p-type inversion MOS capacitor for the top view and cross section respectively. Conventional MOS and inversion MOS capacitors were fabricated monolithically with lateral SiC MOSFETs on n and p-type 4H-SiC epilayers using a commercial CMOS process [7]. The inversion MOS capacitors allow the electrical characterization of the bulk SiO_2 and 4H-SiC/SiO_2 interface in inversion mode [74]. The data show for the first time the C-V characteristics of n and p-type MOS capacitors on 4H-SiC under inversion. The capacitance in the inversion region was determined as a function of frequency and temperature to examine the correlation between inversion capacitance and field effect mobility at high temperatures.

The data in Figures 4.26 and 4.27 show the C-V characteristics for devices with an area of 1.61×10^5 μm^2 for a range of excitation frequencies for n and p-type inversion MOS capacitors normalized to C_{OX} for sample A. The measurements were swept from accumulation

to inversion (Figures 4.26 (a) and 4.27 (a)) and vice versa (Figures 4.26 (b) and 4.27 (b)) at 0.1 V/s in a dark box. The inversion capacitance was measured using a standard procedure where the high terminal was connected to the gate and low terminal (ground) was connected to the body and n^+ or p^+ contact (as electron and hole source). As can be seen from the data in the both Figures 4.26 and 4.27, the capacitance in the inversion region increases with decreasing frequency from 1 MHz to 10 kHz. At 10 kHz, the inversion MOS capacitor demonstrated the typical low-frequency C-V curves due to the attraction of minority carriers (electrons or holes) from the grounded contact (n^+ implanted or p^+ implanted for p and n substrate respectively) when the voltages were applied to the gate contact. It should be noted that no light pulse was applied during the measurement.

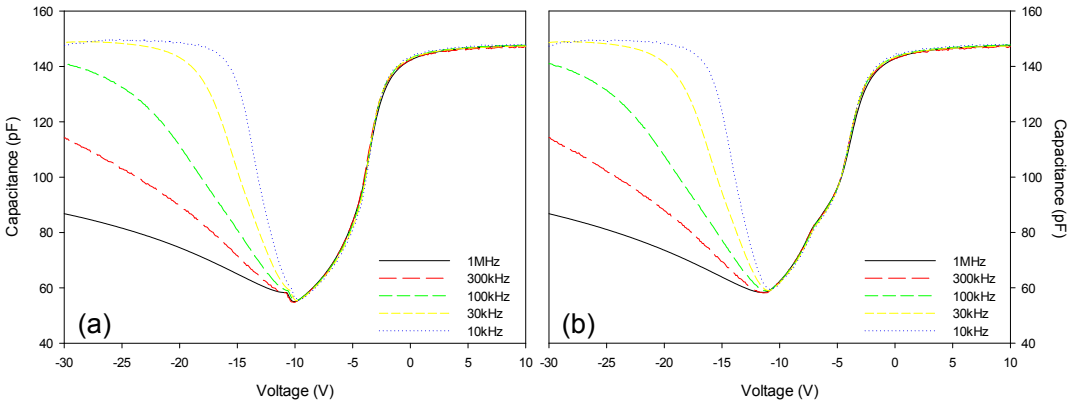


Figure 4.26: C-V characteristics of n-type 4H-SiC inversion MOS capacitor with different frequency from 10 kHz to 1 MHz for sample A at room temperature. The measurements were swept from accumulation to inversion (a) and vice versa (b) at 0.1 V/s in a dark box.

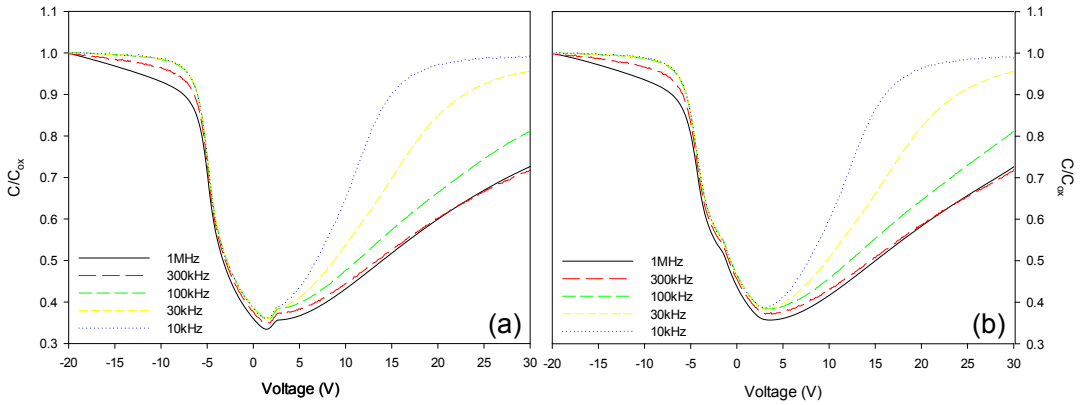


Figure 4.27: C-V characteristics of p-type 4H-SiC inversion MOS capacitor with different frequency from 10kHz to 1MHz for sample A at room temperature. The measurements were swept from accumulation to inversion (a) and vice versa (b) at 0.1 V/s in a dark box.

The data in Figure 4.26 show the C-V characteristics when the measurements were swept

from accumulation to inversion and vice versa for n-type inversion MOS capacitors (sample A). The same C-V characteristics for p-type inversion MOS capacitors can also be observed in Figure 4.27 where the hook and ledge feature appears in the opposite polarity due to the different dopant type. The obvious difference between these two measurements are the hook and ledge feature. When the measurements were swept from accumulation to inversion, a deep depletion hook can be observed which is direct result of interface traps where the minority carriers start to accumulate at the SiO_2/SiC interface and reach equilibrium (charging of surface state or D_{it}). This hook is caused by a barrier against minority carrier flow at the SiO_2/SiC interface [186]. When the measurements were swept from inversion to accumulation, the C-V curve reveals the ledge feature due to the existence of surface states and non-equilibrium behaviour of deep interface traps [186, 223].

The change in inversion capacitance as a function of frequency between 10kHz and 1MHz for both n and p-type inversion MOS capacitors is shown in Figures 4.28 (a) and (b) respectively. As can been seen from the data in both figures, the frequency dependence of inversion capacitance, which is typically observed in Si MOS capacitor, is due to the finite conductivity of the inversion channel and the associated RC time constant (so called minority carrier response) [224, 225]. The inversion properties can be observed when the surface band bending is greater than twice the bulk potential, due to the availability of electrons from the n+ island which surrounds the active area and acts as an external source of minority carriers. This behaviour cannot be observed in conventional SiC MOS capacitor due to the low minority carrier generation.

In the absence of the external source of minority carriers and at room temperature or below, the response of minority carriers is determined by bulk traps of semiconductor. The minority carrier response is important in the inversion region, where the the discrepancy of inversion capacitance between low and high frequency can be observed. For SiC, due to the wide bandgap and associated low intrinsic carrier concentration, the minority carrier response is not observable at room temperature. Three possible mechanisms control the response of minority carriers [114].

1. the diffusion of minority carrier from the semiconductor through the depletion region
2. the generation or recombination of minority carriers in the depletion region
3. external source of minority carriers beyond the gate

These three mechanisms have a strong temperature dependence. Nevertheless, the inversion

properties observed in this work are due to the source of minority carriers from the region that surrounds the MOS capacitor structures.

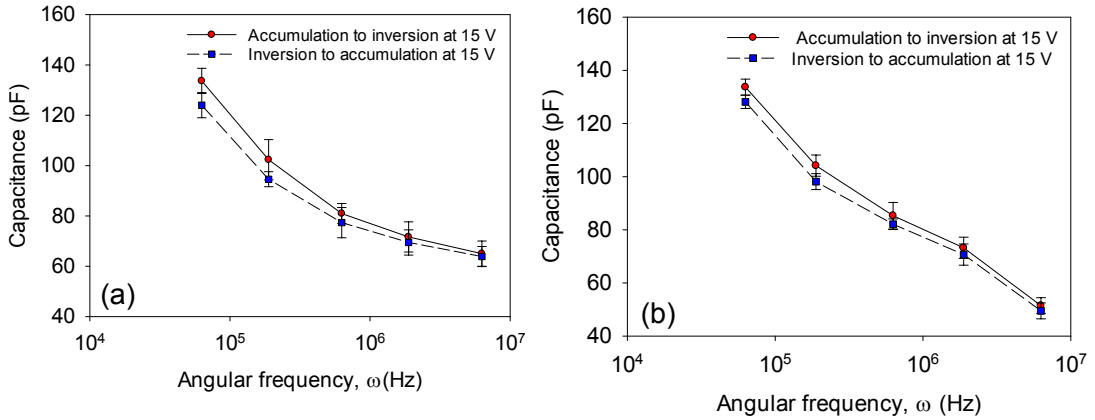


Figure 4.28: The change in inversion capacitance, C_{INV} wth different frequencies at gate votage, V_{G}= 15V for both n and p-type inversion MOS capacitor for sample A at room temperature due to the minority carrier response. The measurements were swept from accumulation to inversion (a) and vice versa (b) at 0.1 V/s in a dark box.

4.7.1 Correlation of inversion capacitance with field effect mobility at RT

Conventional interface state densities are extracted from the data of C-V measurements when biased in the depletion region. In the case of n-channel MOSFETs, a p-type epilayer is used as the starting material. Technically, the interface state density for n-channel MOSFETs needs to be extracted from the C-V measurement of p-type MOS capacitor. However, it is impossible to detect the minority carrier (electron for p-type epilayers) in SiC MOS capacitors in non-thermal equilibrium because of the large bandgap of SiC [114]. Hence, only limited information about n-channel MOSFETs can be provided by analysis of p-type MOS capacitor structures [226]. Alternatively, n-type MOS capacitor has been used to extract the interface state density for n-channel MOSFETs. However, information on interface traps obtained from n-type MOS capacitor is not a direct response from the minority carrier at the SiO_2/SiC interface of n-channel MOSFETs.

In this section, the capacitance under strong inversion conditions of an inversion MOS capacitor was evaluated, instead of interface state density. The correlation between the inversion capacitance with the field effect mobility of the monolithically fabricated MOSFET for n-channel and p-channel with different dielectric formation were analysed at room temperature.

The data in Figure 4.29 show the difference of inversion capacitance at the onset of strong inversion for p-type samples (A, B and C) measured at 1 MHz. A clear minority carrier response can be observed for p-type inversion MOS capacitors. The variation in field effect mobility from n-channel MOSFETs for samples A, B and C were also plotted in the same figure to observe the correlation between inversion capacitance and field effect mobility. As can be seen from the data, a close relation between the inversion capacitance and field effect mobility was observed for the n-channel MOSFETs studied here. It is evident that samples B and C with higher field effect mobility need a lower voltage in comparison to Sample A to achieve higher inversion capacitance, with the lowest mobility sample requiring a higher voltage to not only form the inversion layer but also fill the interface traps. These results suggest that sample A, with the highest interface state density required a higher voltage to form an inversion layer and this results in the observed higher threshold voltage. This result shows that the high interface state density has a significant impact on both the inversion capacitance and field effect mobility. This correlation affirms that the interface state density has degraded the field effect mobility by the reduction of the free carrier concentration in the inversion region [227].

The data in Figure 4.30 show the variation in inversion capacitance at the onset of strong inversion for n-type inversion MOS capacitors for samples A, B and C and the corresponding field effect mobility for p-channel MOSFETs. The difference in minority carrier response that could be observed in the n-type MOSFETs is not obvious for any of the n-type samples. Since the peak field effect mobility for all samples is relatively constant (4-5) cm^2/Vs, there is no discernible relation that can be observed between the inversion capacitance and field effect mobility. This result suggests that the concentration of hole in the inversion region for samples A, B and C is approximately in the same order of magnitude.

4.7.2 Correlation of inversion capacitance with field effect mobility (n-channel) at high temperature

As discussed in the previous section, the main factor that results in the increased drain current and mobility at elevated tempeature is the reduction of trap density that is pertinent to Coulomb scattering. In this section, the inversion MOS capacitors and planar MOSFETS are measured as a function of temperature, up to 400°C, to study the temperature dependence of the inversion capacitance and correlate this with the field effect mobility. The capacitance was measured with an excitation frequency of 1MHz C-V from room temperature up to 400°C.

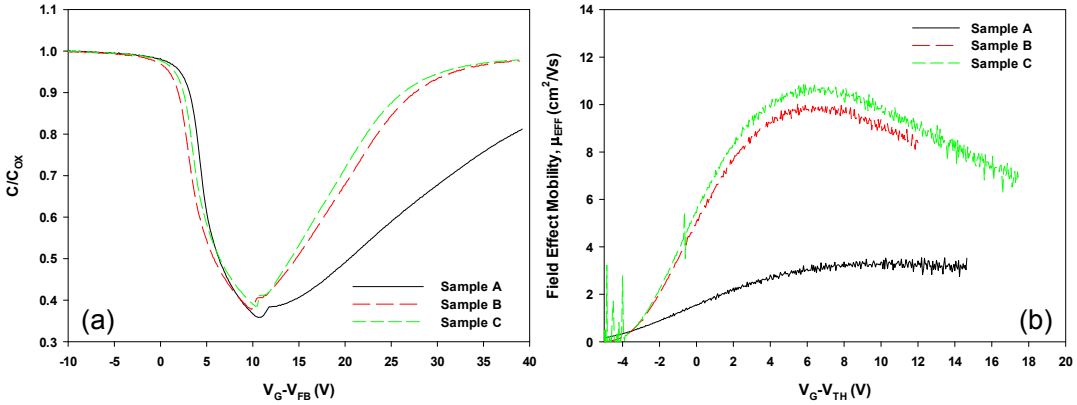


Figure 4.29: (a) Normalized 1 MHz C-V characteristics of p-type 4H-SiC inversion MOS capacitor for samples A, B and C at room temperature. The measurements were swept from accumulation to inversion at 0.1 V/s in a dark box. (b) Comparison of field effect mobility as a function of gate overdrive for n-channel samples A, B and C at room temperature. The size of transistor is L_G=1.2 μm, W_G=200 μm. The field effect mobility was extracted from data of I_D-V_G measured at room temperature with V_D=0.1 V.

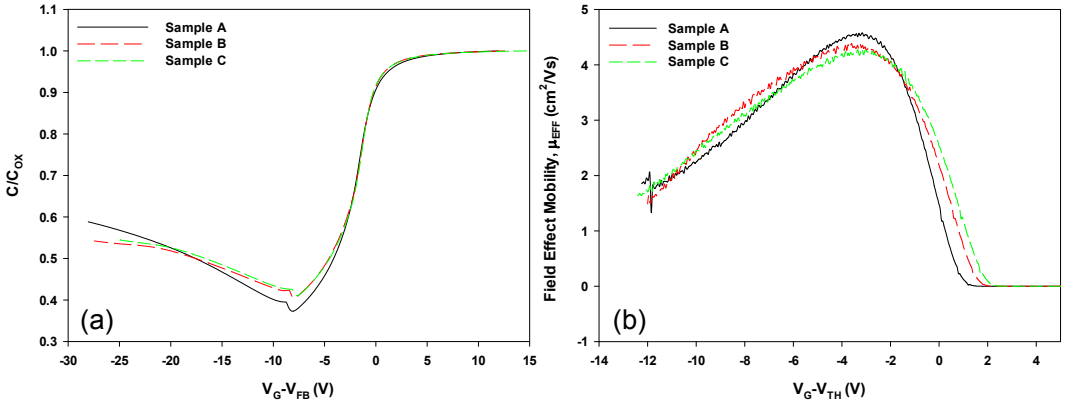


Figure 4.30: Normalized 1 MHz C-V characteristics of n-type 4H-SiC inversion MOS capacitor for sample A, B and C at room temperature. The measurements were swept from accumulation to inversion at 0.1 V/s in a dark box. (b) Comparison of field effect mobility as a function of gate overdrive for p-channel samples A, B and C at room temperature. The size of transistor is L_G=1.2 μm, W_G=200 μm. The field effect mobility was extracted from data of I_D-V_G measured at room temperature with V_D=-0.1 V.

The data in Figures 4.31 (a), (b) and (c) show the changes of inversion capacitance in strong inversion (V_g= 15V) and field effect mobility with temperature for the 3 samples. As can be seen from the data, the inversion capacitance for p-type inversion MOS capacitors increases monotonically with temperature for all samples. The field effect mobility n-channel MOSFETs are plotted on the same axes and they show similar trends with the variation of inversion

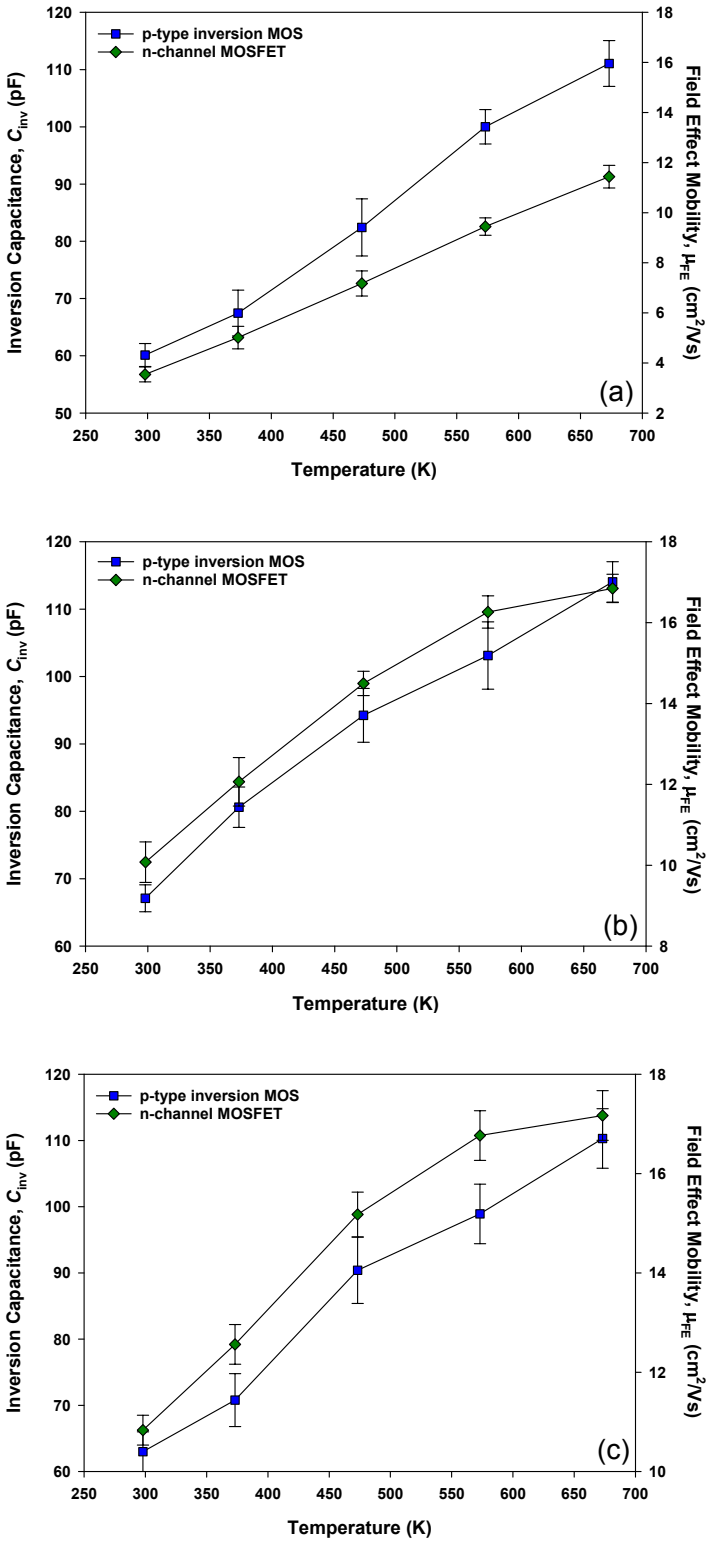


Figure 4.31: The temperature dependence of inversion capacitance (p-type inversion MOS capacitor) at strong inversion and field effect mobility for sample (a) A, (b) B and (c) C (n-channel MOSFET).

capacitance as the temperature changes. This indicates that the field effect mobility of the MOSFETs is correlated with the carrier concentration in the inversion layer for all n-channel MOSFETs studied here. The correlation is strong for p-type inversion MOS capacitor (or N-

channel MOSFET) where the minority carrier concentration (electron) has a strong temperature dependence. As the temperature increases, the trapped charges have sufficient energy to detrap and become free carriers. Hence, more electrons are available to form a channel (increasing the inversion charge) at the interface and this results in a significant increase in the drain current and reduces the subthreshold swing. Furthermore, in silicon, when external minority carriers exist (in this case, surrounding the inversion MOS capacitor), they will a dominant source of minority carriers at all temperatures. As the temperature is increased, the majority carriers concentration increases due to the increase rate of generation and recombination with temperature. However, generation and recombination is unlikely to occur because SiC has a wide bandgap and low intrinsic carrier concentration. The data in Figures 4.31 (a), (b) and (c) agree with the model that the interface trap density is a critical limitation in field effect mobility at elevated temperatures [123]. This result also suggests that the correlation of inversion capacitance with field effect mobility (n-channel) at high temperature works on MOSFETs with different dielectric formation.

4.7.3 Correlation of inversion capacitance with field effect mobility (p-channel) at high temperature

The data in Figures 4.32 (a), (b) and (c) show the changes in inversion capacitance under strong inversion ($V_g = -15V$) and field effect mobility with temperature. For samples A and C, there is no significant change in the inversion capacitance, at temperatures up to 300°C and only a minor increase is observed up to 400°C. In contrast, for sample B, the inversion capacitance for n-type capacitors increases slightly at temperatures up to 300°C but reduces as the temperature increases further. On the same figures, the field effect mobility p-channel MOSFETs are plotted and they show similar trends with an increase in field effect mobility up to around 200°C, and with a slight reduction at 400°C. From these results, it difficult to identify any correlation between the field effect mobility of p-channel MOSFETs and the carrier concentration at the interface. Contrary to the behaviour of electrons, the minority carriers that form the channel in a p-MOSFET have less temperature dependence [228]. As the temperature increases, the occupied trapped charges have sufficient energy to detrap and become free carriers. Hence, a greater number of holes are available to form the channel (inversion charge) at the interface and this results in a significant increase in the drain current. Nevertheless, all the p-channel MOSFETs exhibit an increase in mobility only up to 200°C

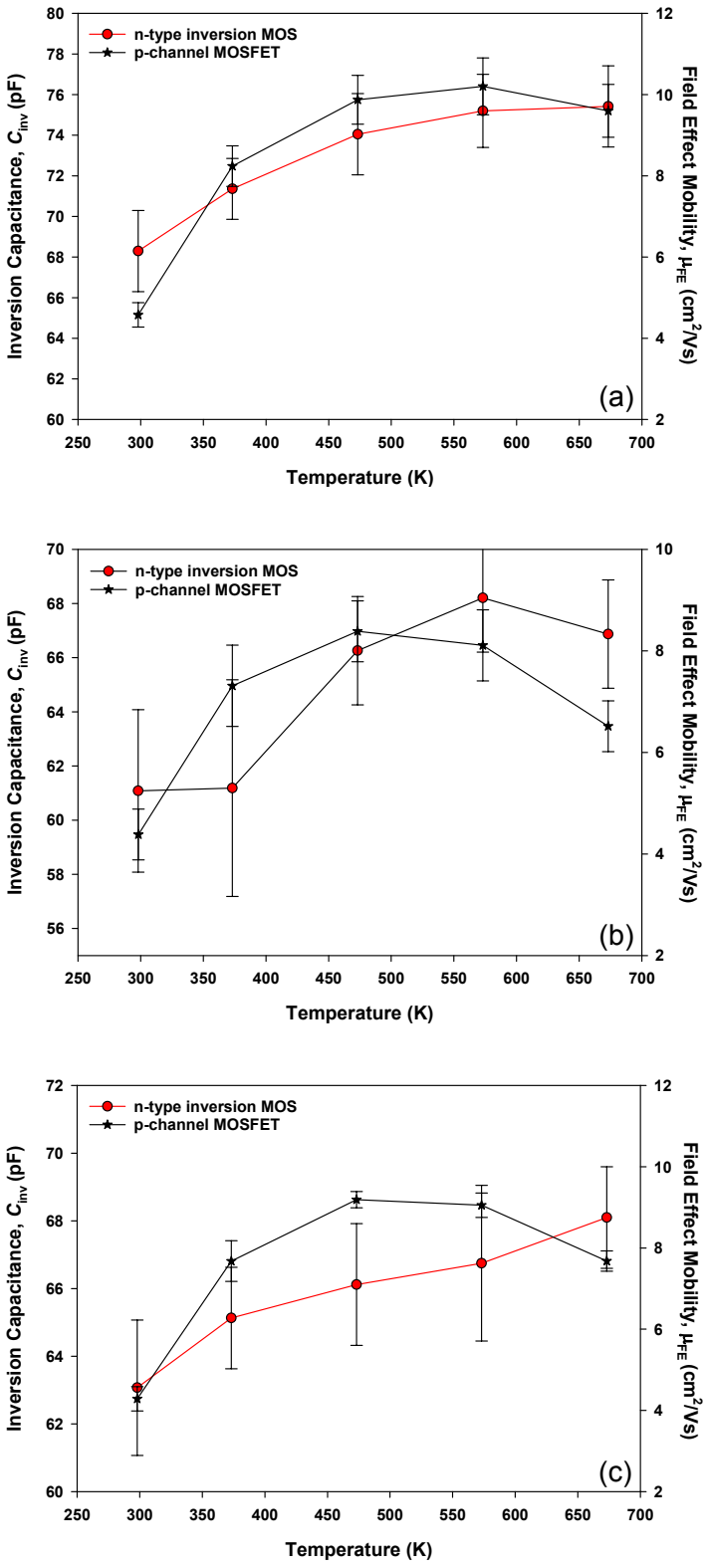


Figure 4.32: The temperature dependence of inversion capacitance (n-type inversion MOS capacitor) at strong inversion and field effect mobility for sample (a) A, (b) B and (c) C (p-channel MOSFET).

The data in Figure 4.31 supports the model that the interface trap density is the critical limitation in field effect mobility at elevated temperatures [123]. This result also suggests

that the correlation of inversion capacitance with field effect mobility (n-channel) at high temperature is independent of the dielectric fabrication process. Therefore, the data show that inversion MOS capacitors are a suitable test structure to study the electrical properties of the 4H-SiC/SiO_2 interface.

4.7.4 Correlation of inversion capacitance with field effect mobility (Discussion)

The data in Figures 4.33 (a) and (b) show the field effect mobility as function of inversion capacitance for n-channel and p-channel MOSFETs respectively. For n-channel MOSFETs, the field effect mobility increased linearly with the increased inversion capacitance for all samples A, B and C. For p-channel MOSFETs, no apparent trend is observed. Coulomb scattering has been proposed as the primary limiting factor for low field effect mobility but from the high temperature measurement data obtained here, the trapped charges are more likely to be responsible. It has been shown that the interface state density of SiC/SiO_2 is high (more that 10^{12} $cm^{-2}eV^{-1}$) and is equivalent to the density of electrons in the inversion region [229]. As shown by the data in Fig 4.33 (a), the inversion capacitance of p-type inversion MOS capacitor increases with increasing temperature, indicating that the trapped charge is thermally activated and starts to detrap at high temperatures. However, as can be seen in Fig 4.33 (b), no clear trend (the uncertainties are significant) can be observed from the correlation of p-channel with the inversion capacitance suggesting that the limiting factor for p-channel field effect mobility is different from n-channel [31, 217].

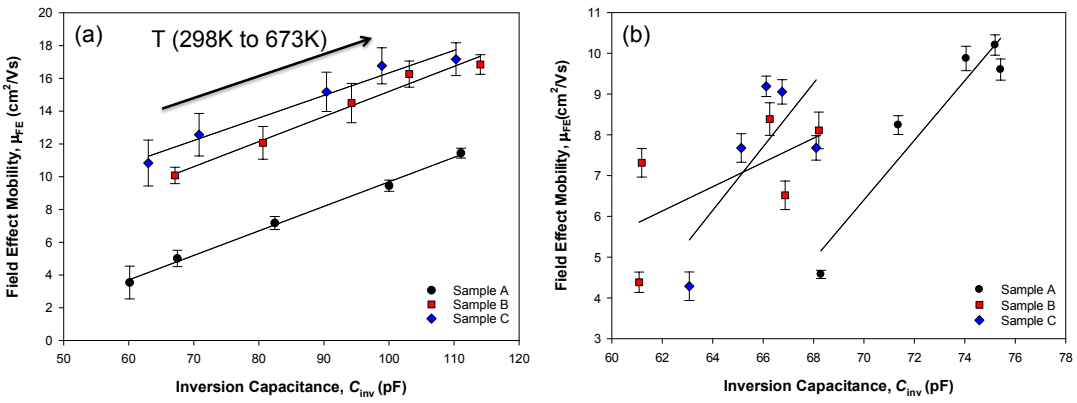


Figure 4.33: The correlation between field effect mobility with inversion capacitance for (a) p-type inversion MOS capacitor/ n-channel MOSFET and (b) n-type inversion MOS capacitor/ p-channel MOSFET.

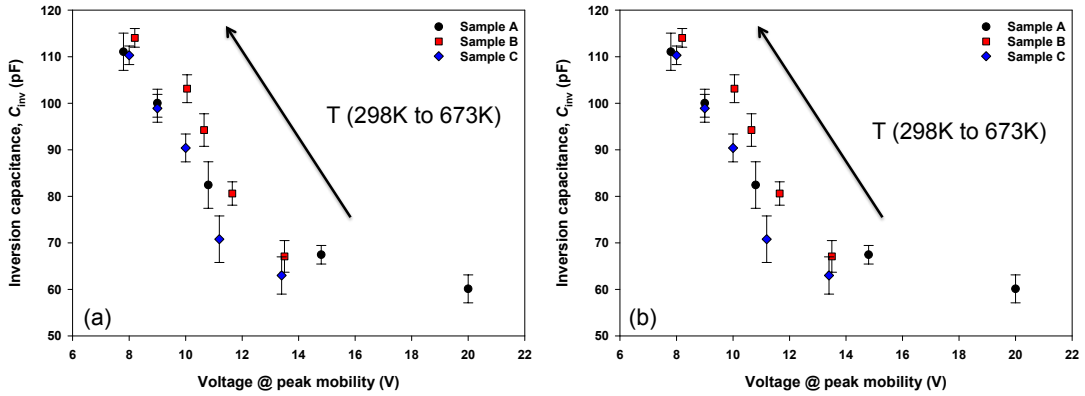


Figure 4.34: (a) Field effect mobility (b) inversion capacitance as a function of voltage at peak mobility.

The data in Figures 4.34 (a) and (b) show the field effect mobility and inversion capacitance as a function of voltage at peak mobility for n-channel MOSFET. The field effect mobility and inversion capacitance increase with the increasing temperature, mainly due to thermally activated charge trapping (de-trapping). At the same time, the threshold voltage at the peak mobility is reduced, resulting from the reduction in Coulomb scattering. The trade-off between field effect mobility and threshold voltage (where as the field effect mobility is increased, the threshold voltage will decrease), are also observed in the literature [64, 113], suggesting that Coulomb scattering and trapped charged play a fundamental role in the behaviour of 4H-SiC MOSFET at high temperatures.

4.8 Summary

Operation of SiC MOSFETs beyond 300°C opens up opportunities for a wide range of CMOS based digital and analog applications. However the majority of the literature focuses only on the optimization of a single type of MOS device (either PMOS or more commonly NMOS) and there is a lack of a comprehensive study describing the challenge of optimizing CMOS devices. This study reports on the impact of deposited oxide performance in non-implanted channel SiC on the electrical stability for both NMOS and PMOS capacitors and transistors. Parameters including interface state density (D_{it}), flatband voltage (V_{FB}), threshold voltage (V_{TH}) and effective charge (N_{EFF}) have been acquired from C-V characteristics to assess the effectiveness of the fabrication process in realising high quality gate dielectrics. The performance of SiC based CMOS transistors were analyzed by correlating the characteristics of the MOS interface properties and transistor up to 400°C. The results from MOS capacitors

comprising interface state density ($D_{\rm it}$), flatband voltage ($V_{\rm FB}$), threshold voltage ($V_{\rm TH}$) for both N and P MOS are in agreement with the expected characteristics of the respective transistors.

The oxide quality, SiO_2/SiC interface properties and leakage current have been characterized by C-V and I-V measurements of the MOS capacitors. Sample C has the lowest, $V_{\rm FB}$ (0.35 V), $N_{\rm EFF}$ (-0.4×10^{11} C/cm^{-2}) and $D_{\rm it}$ (3×10^{12} cm^{2}eV^{-1}), which suggests that the dielectric processing technique produces the best quality of dielectric for n-type MOS capacitors. On the other hand, sample A exhibits the lowest $V_{\rm FB}$ (-5.05 V) and $N_{\rm EFF}$ (1.3×10^{12} C/cm^{-2}) but slightly higher $D_{\rm it}$ (3.3×10^{12} cm^{2}eV^{-1}) for p-type MOS capacitors. In general, the data from $D_{\rm it}$ as a function of energy demonstrates that the reduction of the values of $D_{\rm it}$ for samples B and C on both n-type and p-type of 4H-SiC MOS capacitors. This suggests that the process in sample C would be the most suitable treatment for a monolithic CMOS process in term of reducing $D_{\rm it}$ at the interface of SiO_2/SiC because low $D_{\rm it}$ at the SiO_2/SiC interface may lead to a higher channel mobility [216]. Nevertheless, even having high $D_{\rm it}$ values, the process in sample A display high breakdown voltage on both n-type and p-type of 4H-SiC MOS capacitors. However, further investigation is required to improve the device performance of the MIS system for CMOS applications.

For n-channel MOSFETs, high temperature post gate annealing during the formation of gate dielectric show an increase in interface state density and a reduction of mobility approximately 3 times in comparison to the enhanced standard gate process. This is probably due to the increase in surface roughness in the channel. Nevertheless, the combination of the enhanced standard gate process and high temperature post gate annealing seem effective and results in a lower threshold voltage and slightly higher field effect mobility. In contrast, there is no signficant effect of dielectric formation in field effect mobility for p-channel devices but high temperature post annealing MOSFETs exhibit excellent threshold voltage stability at elevated temperature up to 400°C

The temperature dependence study demonstrated that all MOS capacitor devices (n and p-type) exhibit similar characteristics with stable flatband voltage and a reduction of interface state density with the increasing temperature. This is due to a reduction of the bandgap and detrapping effect that results in a reduction of threshold voltage and an increase in the field effect mobility for MOSFET devices. Nevertheless, the field effect mobility of p-channel MOSFETs only increased with temperature up to 200°C and start to decrease at higher temperature. At temperature higher than 300°C, the effect of detrapping is overwhelmed by

the resistivity of the p-channel.

Finally, an investigation into the device characteristics of inversion MOS capacitor was performed to find the correlation between inversion capacitance and the field effect mobiltiy. It was found that as the temperature increases, the field effect mobility of both n-type and p-type also increase, due to an increase in inversion charge and a reduction of the trapped charge. At room temperature, the correlation between inversion capacitance and the field effect mobility is excellent for n-channel devices. Nevertheless, no significant trend was found for p-channel MOSFET; a of similar field effect mobility was shown by all gate dielectric formation process. The correlation between inversion capacitance and the field effect mobility at elevated temperature was also found in n-channel MOSFETs and the limiting factor for field effect mobility is discussed. This results from the inversion MOS capacitor are useful to understand the operation of 4H-SiC devices over a broad range of temperatures in order to aid the advancement of CMOS process for high temperature digital and analogue applications.

Chapter 5

3D Structures for Silicon Carbide Transistors

5.1 Fabrication and characterization of 3-Dimensional MOS capacitors 4H-SiC by PECVD as gate dielectric

The characteristics of 3-Dimensional 4H-SiC MOS capacitors fabricated using reactive ion etching are described. 4H-SiC MOS capacitors with different trench sizes were fabricated and studied by scanning electron microscope. An enhanced accumulation oxide capacitance, C_{OX} has been observed on 3-D MOS capacitors in comparison to planar MOS capacitors. The increase of oxide capacitance, C_{OX} is proportional to the increase of surface area of the 3-D MOS capacitors. Nevertheless, the increase of C_{OX} deviates from the theoretically calculated oxide capacitance due to the anisotropic deposition rate of SiO_2 on trench structures by plasma enhanced chemical vapour deposition (PECVD) as reported in [127].

Three samples with different dielectric formation (post-oxide annealing) have been studied to observe the changes in the electrical characteristics of the MOS capacitors. The characteristics of 3-D MOS capacitors, such as the flatband voltage (V_{FB}), effective oxide charge (N_{EFF}), and interface state density (D_{it}) with a different number of trenches and different sidewall planes were also investigated. The proposed approach can be utilized to fabricate high-performance 4H-SiC MOSFET or high-sensitivity gas sensor.

Silicon carbide metal-oxide-semiconductor transistors have been a remarkable component in power modules in automation, industrial machines and home appliances [19]. In comparison to conventional devices, SiC-MOSFETs have demonstrated a significant reduction in power loss due to the low on-state resistance. 4H-SiC is capable of providing excellent performance for high voltage, high frequency, high temperature and high power devices which leads to increased efficiency and reliability of power electronics systems due to its superior material properties such as wide bandgap, high electrical breakdown voltage and high thermal conductivity [6]. This emerging technology has made rapid progress in the last decade and it is expected to play an important role in energy saving and emission reduction. However, the field effect mobility in SiC MOSFETs is still low (only about 4% of the bulk mobility) in comparison to silicon MOSFETs (50% of the bulk mobility) due to high defect density at the SiC/SiO_2 interface. To

fully utilize the properties of SiC, several methods have been considered to reduce the interface state density and increase the mobility [80, 89, 102]. One of the attractive approaches is that of a multigate MOSFET that is capable of increasing the drain current, minimizing short channel effects and improving electrostatic integrity [127]. The multigate structure can be applied to SiC complementary metal-oxide-semiconductor (CMOS) and MOS sensors, as well as relating to power devices [137].

The FinFET structure provides a viable route to alleviate challenges relating to electrical performance and power consumption [230]. In silicon technology, Fin / 3D structure is used to suppress short-channel effects such as threshold voltage roll-off, drain induced barrier lowering and subthreshold swing (S) [231]. In SiC technology, it also provides higher carrier mobility (due to higher inversion mobility on $(11\bar{2}0)$ or $(1\bar{1}000)$ sidewall), especially at gate voltages near the threshold voltage, because they occupy less area than planar MOSFETs and multiple fin heights also can be achieved rather easily [127, 132]. The fin structure has the potential to be extremely promising for silicon carbide field effect transistors. This is because higher inversion mobility on the sidewall such as $(11\bar{2}0)$ and $(1\bar{1}000)$ plane in comparison to (0001) plane effectively increase the drain current per channel area. The drain current and gate control of a 3-D structure can be improved by the sidewall and corner effect respectively as reported in previous research [231, 232]. However, due to its hardness and high bond strength of SiC which makes it resilient to harsh environments, wet etching has been proven not to be feasible in order to pattern SiC [21, 233]. This has become an obstacle for the fabrication of 3-D structures in SiC technology because this property makes it difficult to be etched in typical acid or base solutions. Indeed the only techniques for chemical etching of SiC employ molten salt fluxes, hot gases, electrochemical processes or plasma etching. For these reasons, most attention is now focussed on dry etching methods for SiC, which have been developed for high power, high temperature electronics. RIE and ICP are viable processes that can be implemented to pattern SiC. Even having low etch rates (typically hundreds of angstroms per minute), RIE is capable of producing highly anisotropic features with little undercutting or micro trenching [139]. The key to having a smooth surface is the realisation of sharp, smooth edges on masking features. In a SiC MOSFET, the interface between the SiC and the gate dielectric is crucial for the device performance. Physical damage to the trench and the resulting formation of a high density of interface states will result in a low inversion channel mobility [234] and poor oxide quality. Besides the oxide quality, 3-D MOS structures also require conformal step coverage of the gate oxide.

In order to exploit the benefits of new structures for MOSFETs, it is important to understand

the limitations of 3D MOS capacitors. In this study, 3-Dimensional MOS capacitors with a different number of trenches were fabricated using RIE. The 3-D gate structures of MOS capacitors were investigated by scanning electron microscope (SEM). The characteristics of 3 Dimensional MOS capacitors, such as flatband voltage (V_{FB}), effective oxide charge (N_{EFF}) and interface state density (D_{it}) were studied. Within this work, the performance of 3-Dimensional MOS capacitors on different off-angles were also reported. Moreover, the effect of incorporating nitrogen and hydrogen by post-oxide annealing in N_2 and forming gas are discussed based on flatband shift and interface state density. The proposed approach can be utilized to fabricate high-performance MOSFETs for logic circuit and sensor applications.

5.1.1 Device fabrication

A dedicated mask set has been designed to enable the simultaneous processing and characterization of planar and 3-D capacitors. As shown in Fig 5.1, two types of planar MOS capacitors were fabricated; non etched and etched. The non etched planar MOS capacitors are protected / covered with a metal mask during the etching process, where the non etched planar MOS capacitors are open / not covered. This is to study the effect of the etching process to the device characteristics in regard to the surface damage that will result in higher interface trap density. For the 3-D MOS capacitors, different trench sizes on the top and bottom trenches. As the trench sizes are reduced, the surface area of the 3-D MOS capacitors is increased due to the contribution from the sidewalls area. The 3-D MOS capacitors are also fabricated with different off angles from 0° to 90° at each 15° to investigate the effect of different sidewall plane to the characteristic of MOS capacitors such as flatband voltage, V_{FB}, effective oxide charge, N_{EFF} and interface state density, D_{it}.

Fig 5.2 shows the process flow for the fabrication of 3-D MOS capacitors. 4° off angle 4H-SiC samples with a nitrogen concentration of 5.8 $\times$ 10^{15} cm^{-3} were used as the starting material. A Ti (5 nm) / Nickel (100 nm) layer was deposited by e-beam as a mask layer for the etching process. RIE was used to form the 3-D / trench structure on the epilayer. After the removal of the metal mask and sample cleaning, SiO_2 with a thickness of 30 nm was deposited by plasma enhanced chemical vapour deposition (PECVD) with power of 20 W using N_2O, SiH_4 and N_2 at 350°C. Subsequently, the samples were annealed at 1000°C for 10 minutes in N_2 gas environment to densify the oxide. Then, a stacked metal of Ti (5 nm) / Nickel (100 nm) was deposited to form the back contact using e-beam evaporation. The samples were subsequently annealed for 200 s at 1050°C with flowing forming gas (100 sccm) to form nickel silicide based

Ohmic contact. Finally, aluminium was employed as a gate metal with size area of 200 μm $\times$ 200 μm. Pysical vapour deposition (PVD) was used to deposit the metal gate in order to get conformal coverage of metal deposited on the top, bottom and sidewall of the structure.

5.1.2 Result and Discussion

Fig 5.3 shows SEM images of a) the surface roughness on the sidewall of the trench structure, b) the 3-D MOS capacitor prior to metallisation, c) the cross section of the 3-D MOS capacitor and d) the metal coverage on the trench structure. The 3-D gate structures were formed

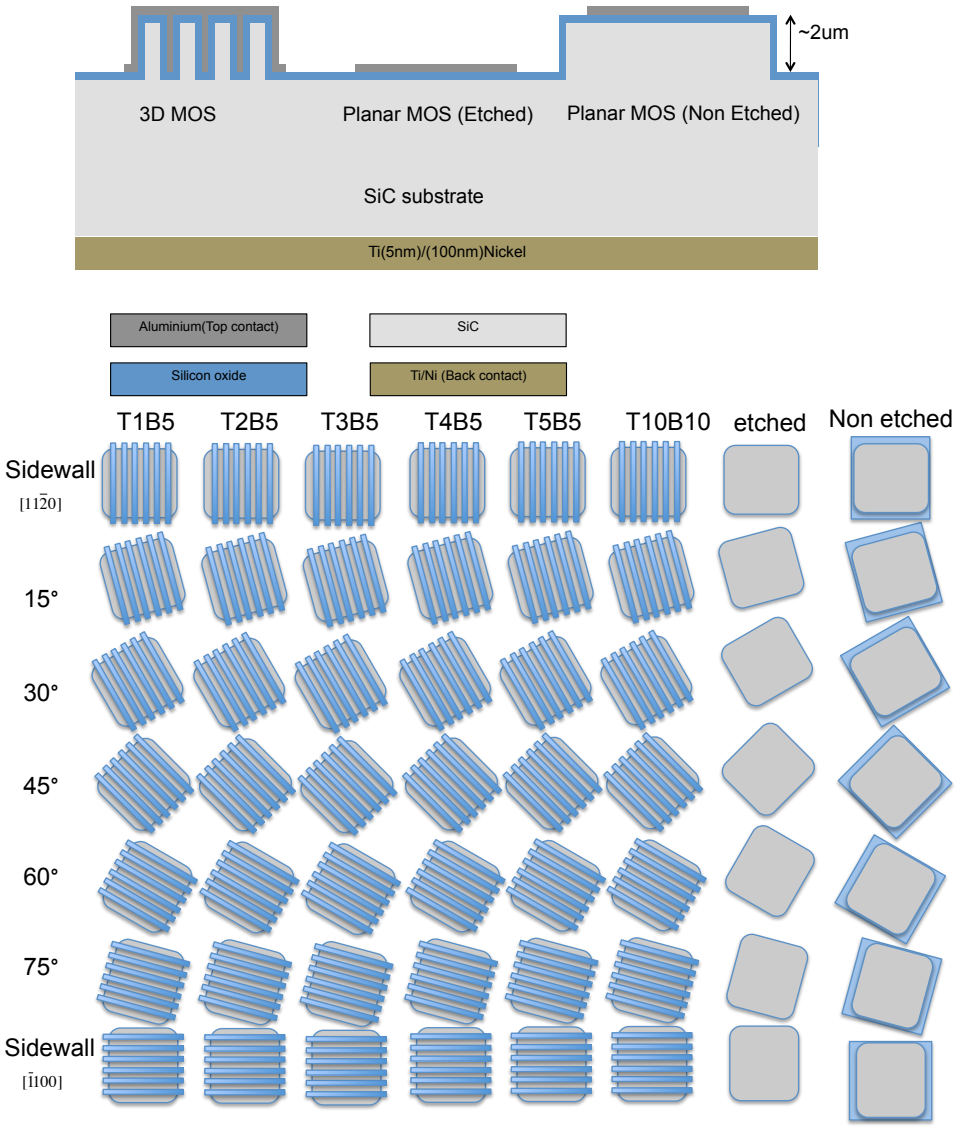


Figure 5.1: Schematic diagram of the cross-section of 3D MOS capacitors (top) and the illustration of mask design for 3-D MOS capacitors (below).

with a negligible micro-trenching and low surface roughness on the sidewall. The images show that the 3-D gate structures of the 4H-SiC MOS capacitors were succesfully fabricated with excellent trench profile and metal coverage. The size of the 3-D / trench sizes of MOS capacitors, top (T), bottom (B) and height (H) used in the following discussions are summarized in Table 5.1. For example, T10B10 is a 3D MOS capacitor with the top finger having a width of 10 μm and the bottom of the trench of 10 μm. The height of the 3-D trench structures were fixed at 3 μm.

The additional area on the sidewalls 3-D structures increases the active area for the MOS

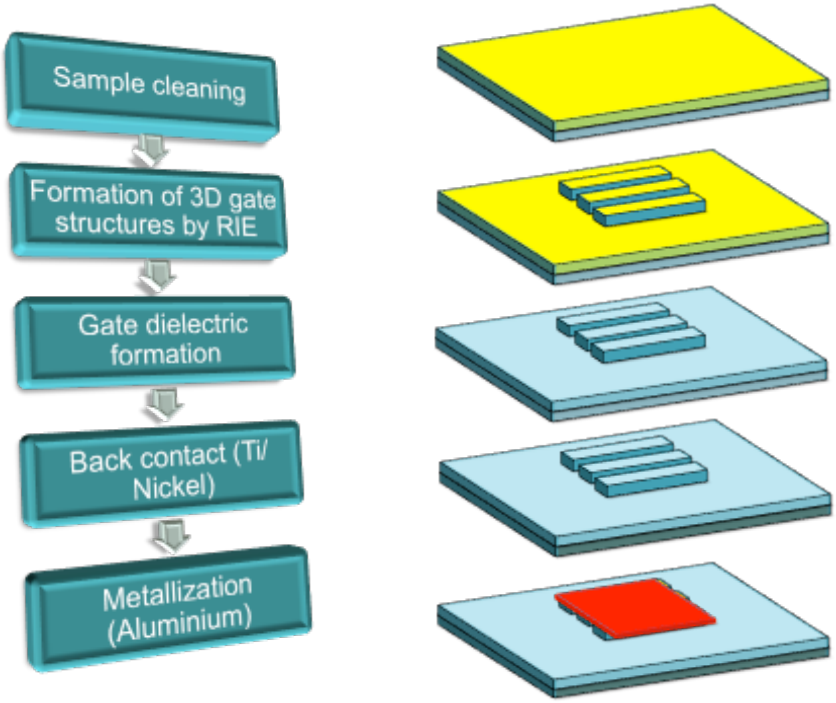


Figure 5.2: Process flow of the fabrication of 3-D MOS capacitors.

Table 5.1: Summary of the size parameters for 3-D MOS capacitors.

Sample name	Total Surface Area (μm^{-2})	Description
Planar (non-etched)	400	planar MOS capacitor
Planar (etched)	400	planar MOS capacitor
T10B10	508 (27%)	Top=10 μm, Bottom=10 μm
T5B5	616 (54%)	Top=5 μm, Bottom=5 μm
T4B5	640 (60%)	Top=4 μm, Bottom=5 μm
T3B5	664 (66%)	Top=3 μm, Bottom=5 μm

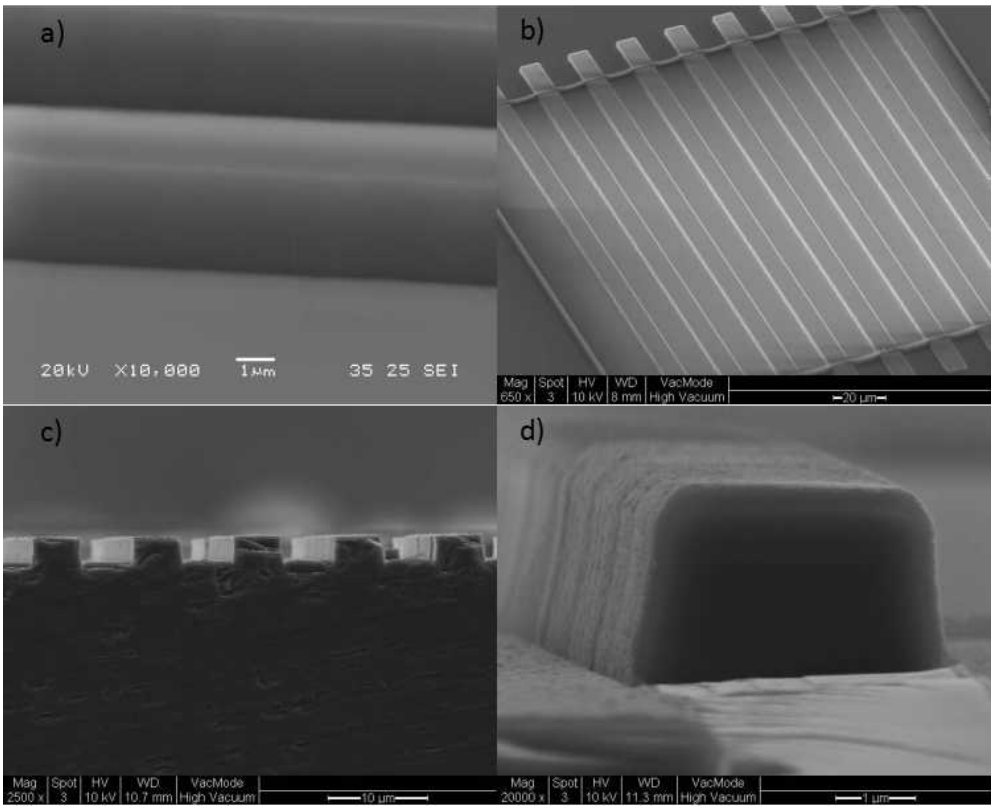


Figure 5.3: SEM images of a) Surface roughness of trench on sidewall, b) 3-D MOS capacitor before metallization, c) Cross-section, d) 3-D trench after metallization.

capacitors and consequently results in higher oxide capacitance as described by Equation 5.1.

$$C_{\mathrm{OX}} = \frac{\varepsilon_s \varepsilon_o A}{T_{\mathrm{OX}}} \tag{5.1}$$

The electrical measurements were performed using a Keithley 4200 parameter analyser and a Cascade Summit probing station. In all measurements, the voltage was swept from accumulation region to depletion region and vice-versa at rate of 0.1V/s. Fig 5.4 depicts the C-V characteristics of 3-D 4H-SiC MOS capacitors with different trench sizes. The oxide capacitance, C_{OX} of the 3-D MOS capacitor increased with the number of trenches or surface area as described by Equation 5.1. Fig 5.5 shows the parallel-mode conductance, G_{P} measured at 1 MHz on different of 3-D MOS capacitors. The conductance peak increases in magnitude and becomes broader as the surface area increases. The relation of oxide capacitance, C_{OX} with surface area was studied by comparing experimental and data with theoretical predictions using Equation 5.1. As can be seen from the data in Fig 5.6, the experimental oxide capacitance is higher than the theoretical predictions. The origin of this discrepancy is the deposition profile of the PECVD SiO_2 that results in thinner gate oxide on the sidewall, in comparison to that on

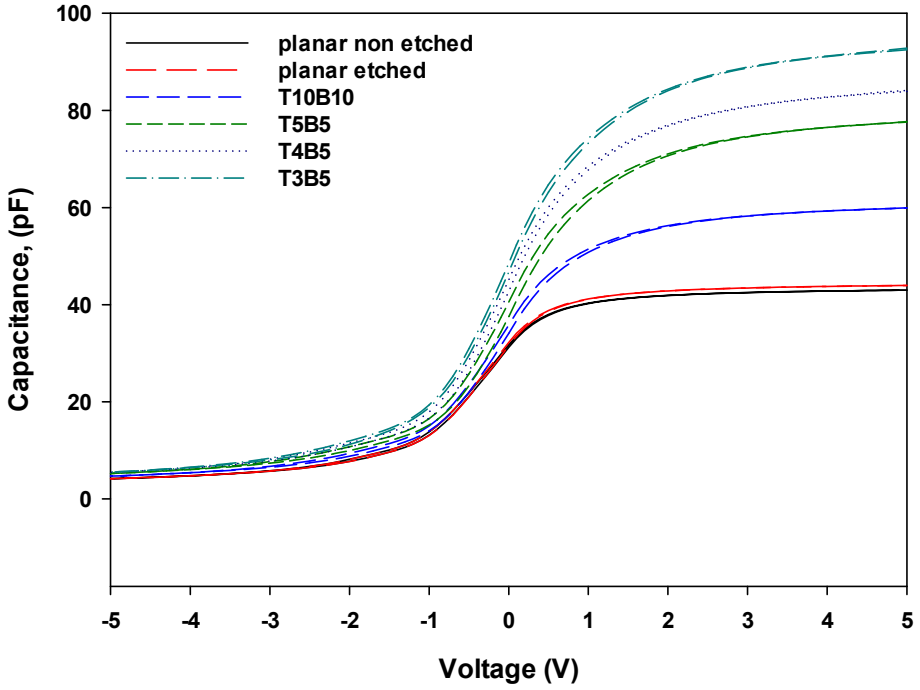


Figure 5.4: C-V curves of 3-D MOS MOS capacitors with different trench sizes measured at 1 MHz. For example, T10B10 is a 3D MOS capacitor device with a width of 10 μm on the top and bottom trench.

the top plane [127]. The gate oxide thickness on the sidewalls can be estimated by Equation 5.2.

$$C_{\mathrm{OX,Total}} = \frac{\varepsilon_s \varepsilon_o A_{\mathrm{Planar}}}{T_{\mathrm{ox,Planar}}} + \frac{\varepsilon_s \varepsilon_o A_{\mathrm{Sidewall}}}{T_{\mathrm{OX,Sidewall}}} \tag{5.2}$$

The data in Fig 5.7 show the increase of oxide capacitance, ΔC_{OX} with increased surface area, ΔA from the sidewall of trench structures. From this analysis, an oxide thickness of $\sim$20 nm was determined on the sidewall of 3D-MOS capacitors. The ratio of the thickness of the gate oxide on the sidewall to the gate oxide on the planar is about 0.67, which is in good agreement with data published in [127].

Fig 5.8 shows the interface state density as a function of energy for planar and 3-D MOS capacitors extracted using the Terman method. There is no significant difference in the interface state density for planar non-etched and etched planar MOS capacitors, however, the D_{it} of 3-D MOS capacitors increased with the sidewall area in MOS structures. The origin of the additional D_{it} in 3-D MOS capacitors may be due to the damage induced on the sidewalls and trench corners of 3-D structure during the etching process. This indicates that the etching process has produced more significant damage on the sidewall in comparison

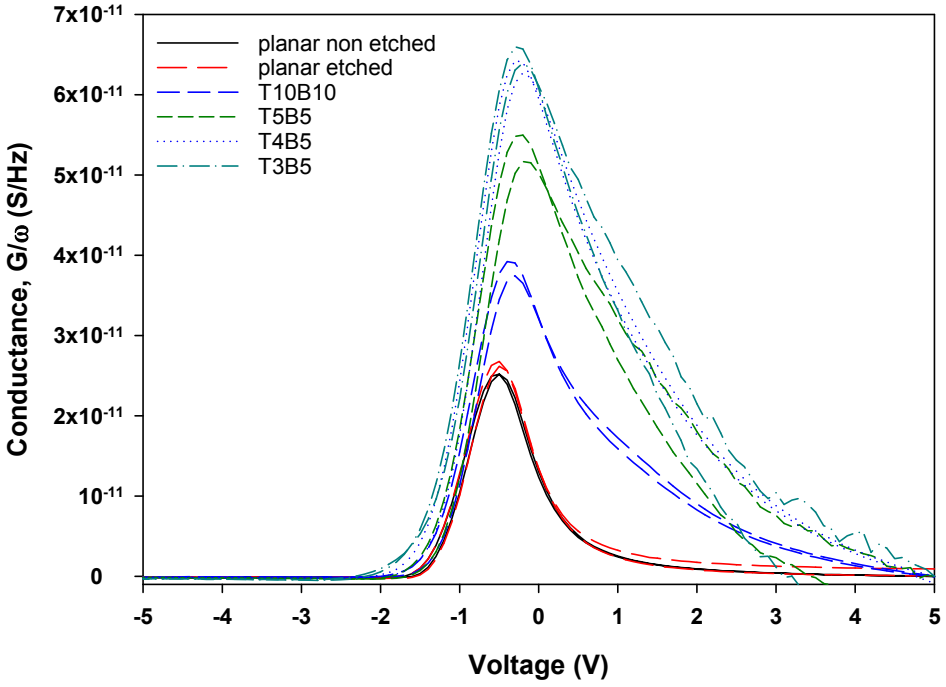


Figure 5.5: G-V curves of 3-D MOS MOS capacitors with different trench sizes measured at 1 MHz.

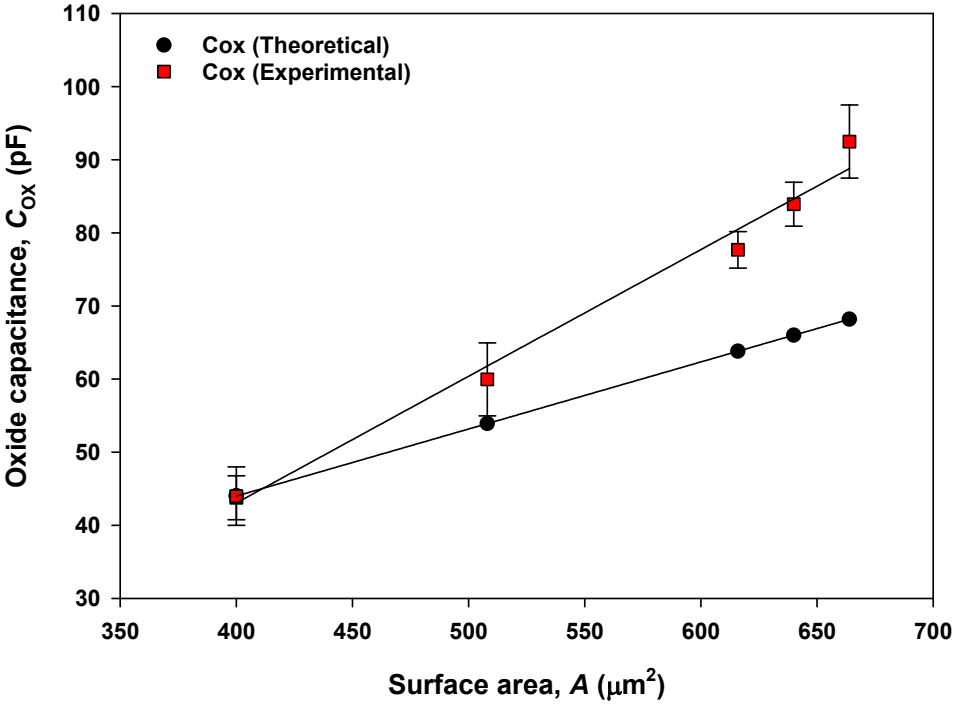


Figure 5.6: Changes of oxide capacitance, C_{OX} (accumulation region) with different the trench sizes.

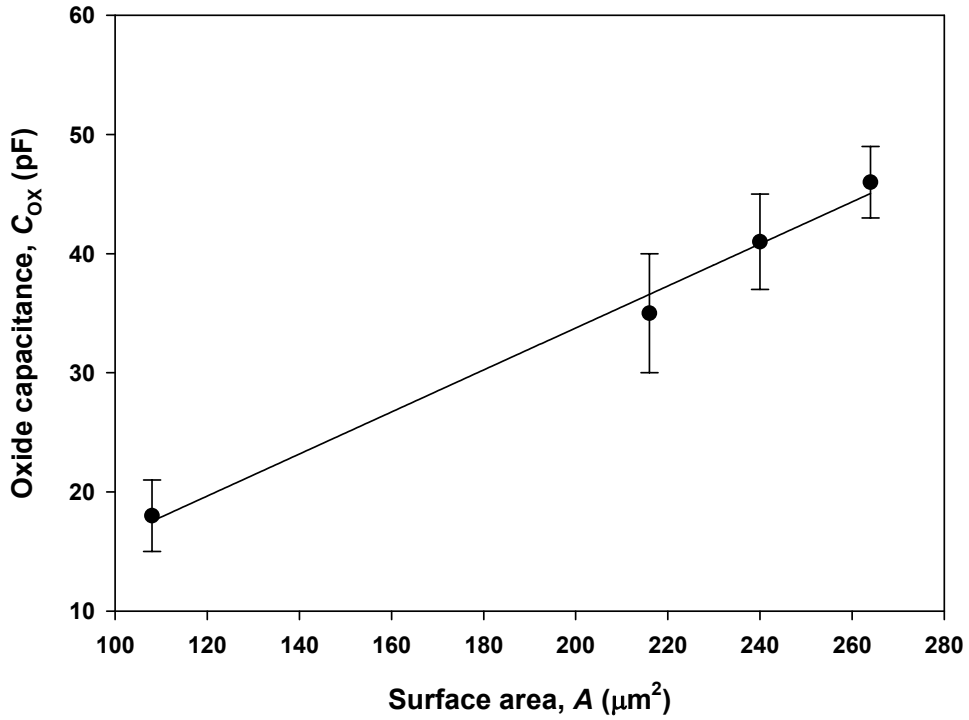


Figure 5.7: Increment of oxide capacitance, $\Delta C_{\rm OX}$ with additional area on the sidewalls.

to the planar surface. The flatband voltage, $V_{\rm FB}$ of the 3-D MOS capacitors are slightly larger (approximately 0.1 to 0.2 V) in comparison to the planar MOS capacitors which were both -0.2 V. The effective oxide charge, $N_{\rm EFF}$ of 3-D MOS capacitors is slightly lower with a value of 4 to 5 $\times$ 10^{11} cm^{-2} in comparison to planar MOS capacitors with a value of 6 $\times$ 10^{11} cm^{-2}.

5.1.3 3-D MOS capacitors with different off angles

It has been reported that different planes on SiC exhibit different characteristics of surface roughness and interface state charge [50]. In order to study the effect of incorporating different sidewall planes in 3-D MOS structures, the electrical characteristics were investigated using C-V and Conductance-Voltage (G-V) techniques. The oxide capacitance, $C_{\rm OX}$ of the 3-D strucuture with different off angles are shown in Fig 5.9 for four of the structures described in terms of their physical trench dimensions. However, the data show no sidewall planes dependence on the $C_{\rm OX}$ as the oxide capacitance, $C_{\rm OX}$ are almost the same across different sidewall plane of 3-D MOS capacitors as the capacitors are rotated at each 15° with different off angles from 0° to 90°. The flatband voltage and effective oxide charge of 3-D MOS

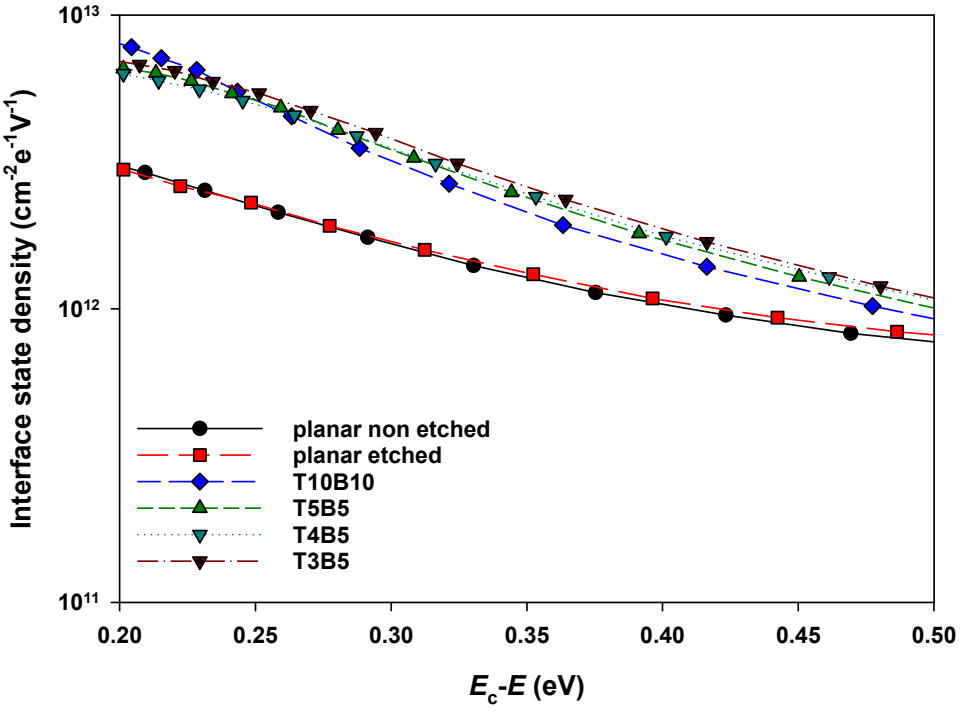


Figure 5.8: Interface state density as a function of energy of 3-D MOS capacitors with different trench sizes.

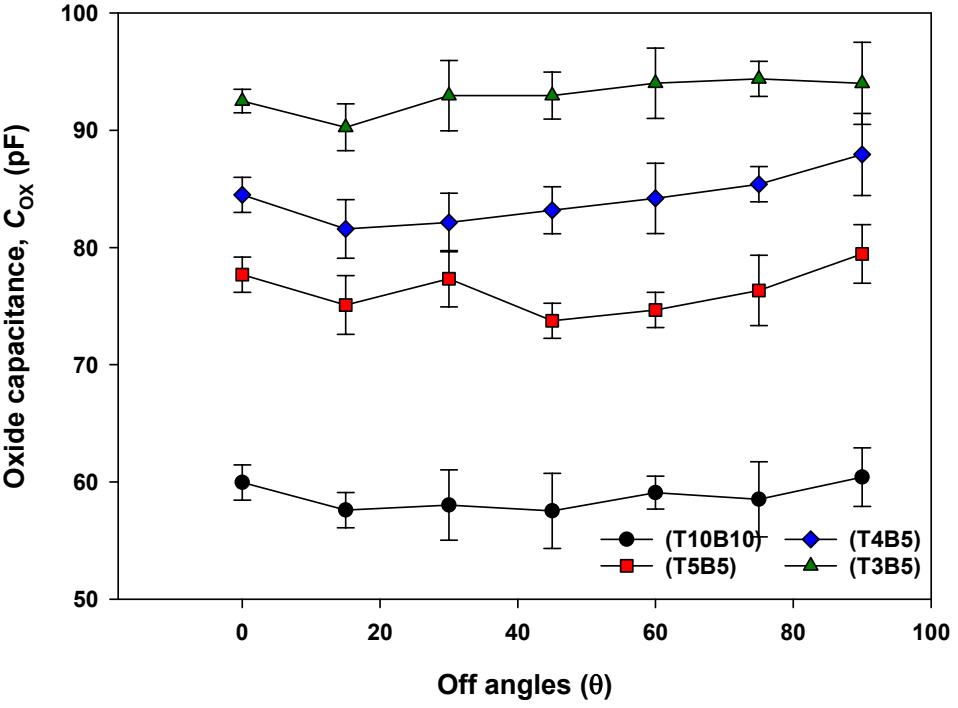


Figure 5.9: Oxide capacitance of 3-D MOS capacitors on different off angles.

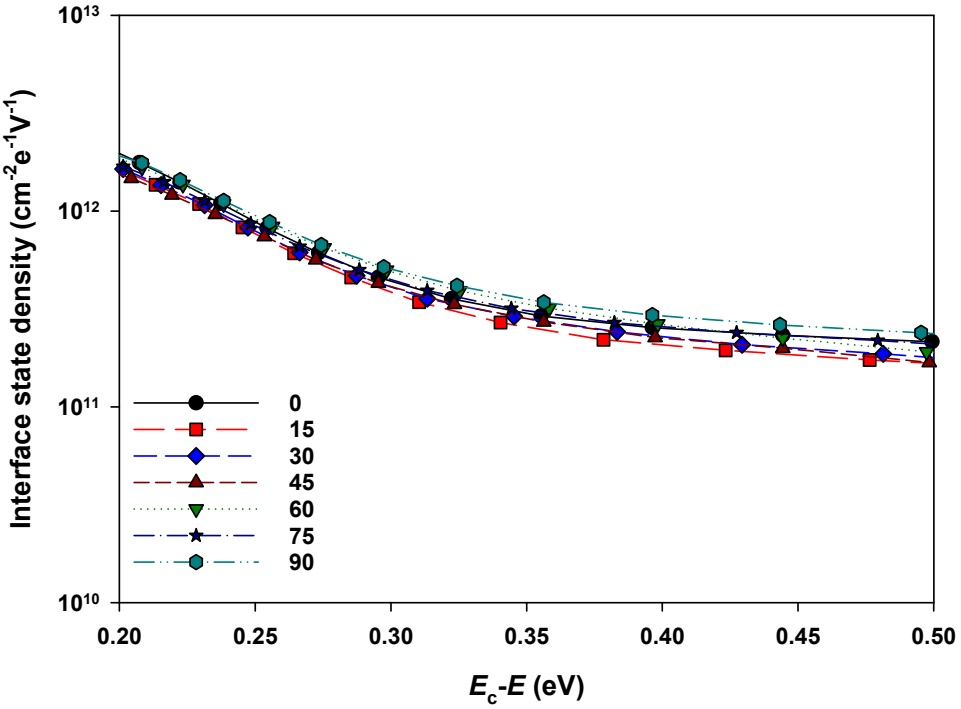


Figure 5.10: Interface state density as a function of energy for 3-D MOS capacitors on different off angles extracted using Terman method.

capacitors do not show significant variation with different sidewall planes with values between 0.1 and 0.2 V and 5 and 6 $\times$ 10^{11} cm^{-2} respectively. The data in Fig 5.10 show the interface state density as a function of energy for 3-D MOS capacitors fabricated on different sidewall planes extracted using the Terman method. The dependence of different sidewall planes on the inteface state density is within the uncertainty in the data. Data reported in literature suggest that [58, 124, 235] the interface state density on the sidewall planes such as $(11\bar{2}0)$ plane and $(1\bar{1}00)$ are lower, but there is no significant change in the interface state density observed in the data. This is might be due to the 4° off angle of the starting material that results in the sidewalls not being fully aligned with the crystallographic planes. This is also due to the fact that characteristics of the 3-D MOS capacitors are not based on planes on the sidewalls, they are the combination of planar and the sidewall orientations. This is to be expected for devices manufactured on commercial wafers. The trench structures formed using RIE consist of surfaces that deviate from the perfect/ideal sidewall orientations resulting in a complicated morphology. Furthermore, the characteristics of the planar planes which are dominating the enhanced capacitance of the 3-D MOS capacitors and might result in similar device characteristics even when the capacitors are rotated to different off angles. The damage created during RIE process to form trench structures can also be considered as a factor for high

density of interface states that gives rise to anomalous electrical behaviour.

5.2 3-Dimensional 4H-SiC MOS capacitors grown by atomic layer deposition of Al_2O_3

The move to nanoscale transistors has been the key enabler in the realisation of high performance electronic systems. In order to facilitate the continued reduction in physical dimension of devices to the nanometer scale, 3-D structures, in the form of FinFETs [236] are an area of active research in silicon technology in order to minimise short channel effects. These 3-D structures are often formed by etching features in the surface of the semiconductor to form devices (that include the sidewalls) which result in higher levels of gate control and hence enhanced performance. However, silicon technology cannot function in environments where the temperature exceeds 175 °C, as commonly found in a wide range of industrial applications. In these environments, 4H-SiC has become the most suitable candidate for next generation electronic devices for deployment in extreme environments [5, 58] because of the chemical stability of the carbon – silicon bond. The hexagonal crystal structure of silicon carbide results in significantly different surface chemistry of the sidewalls in comparison to the planar (0001) surface – a situation that does not occur in silicon. Hence, the realisation of nanoscale 3-D transistors in silicon carbide is a greater challenge than in silicon because of the influence of the chemistry of the sidewall.

The demand for high performance, miniaturised resilient electronic circuits operating in environments where the temperatures exceed 300°C has grown significantly in the last few years, with SiC offering solutions due to its superior electrical properties [148, 237]. At present 4H-SiC devices with gate lengths in excess of 1 μm have been used to demonstrate simple circuits in automation, aerospace and home appliances [19]. The challenge of maintaining the electrostatic integrity of a short channel MOSFET at high temperatures has limited the aggressive scaling of silicon carbide devices, however the enhanced control of the 3D gate structure in a FinFET could mitigate this, leading to significant potential enhancements in performance for high temperature logic circuits.

For the multi–μm scale MOSFETs being researched at the present time, one of the main technological concerns in 4H-SiC technology is that of electrically active defects at the SiO_2/ SiC interface, leading to a high density of interface states (D_{it}) near the conduction band edge, resulting in low effective inversion channel mobility [67, 111]. This appears to reduce the current capability of 4H-SiC MOSFETs, which means that the performance is below

that predicted theoretically. The effective mobility is reduced by Coulombic scattering by trapped charges [141], interface states and fixed oxide charges, which decreases the number of free carriers in the channel [113]. The reported [48, 147, 238] channel mobility in 4H-SiC MOSFETs has increased due to the development of post-oxidation annealing techniques using nitrogen [58] and phosphorus [59], which act to passivate defects at the SiO_2/SiC interface. However, the extracted mobility characteristics are still significantly lower than the technical capability of the material, so further improvements are still required to realise the true potential of the technology.

In power device technology, an attractive approach to increase the channel mobility is to use a vertical trench MOSFET structure which utilizes the sidewall of the trench, typically the $(11\bar{2}0)$ face, to enhance the drain current and improve gate control [58, 235]. The vertical trench power MOSFET structure produces good device performance with high channel density and low resistance. It is well known that different surface orientations of 4H-SiC have anisotropic electrical properties and show differing oxidation rates and surface roughness values. An enhanced drain current has been demonstrated by the use of a 3-D gate structure power MOSFET owing to the anisotropic mobility properties of 4H-SiC on different planes. This indicates that the development of 3-D structures offers a route to high performance nano–scale devices that are capable of operating in high temperature environments, because 3-D gate MOSFETs have better control of short–channel effects [127, 132].

The inability to control the threshold voltage in FinFET structures in a manner similar to that of a planar MOSFET is a critical challenge in the realisation of nanoscale transistors in materials such as silicon carbide. Hence, a systematic study is required to identify the effect of the sidewall surface on the device characteristics, which is vital if this technology is to be used for nanoscale devices.

One of the challenges in fabricating FinFET structures is the etching process to realise the 3-D gate structure which might cause damage to the surface and result in a high interface state density [234]. In this study, 3-D MOS capacitors have been fabricated on 4H-SiC, alongside planar (etched) and planar (non-etched) structures, as shown in Figure 5.11, to investigate the effect of the 3-D gate structure on the characteristics of the gate capacitor (the critical part of a MOSFET device). As the surface area of 3-D MOS capacitors is larger in comparison to the conventional planar capacitor on the same footprint, it is expected that 3-D MOS capacitors will give higher capacitance compared to the planar capacitor. The planar capacitors on etched and non-etched surfaces act as a reference to understand the characteristics of the trench bottom

and top surface of the finger that comprise the 3-D MOS capacitors. 3-D MOS capacitors with different sidewall planes were also investigated, by rotating the angle of the etched fingers on the wafer surface in multiples of 15° with respect to $(11\bar{2}0)$.

5.2.1 Experiment and evaluation method

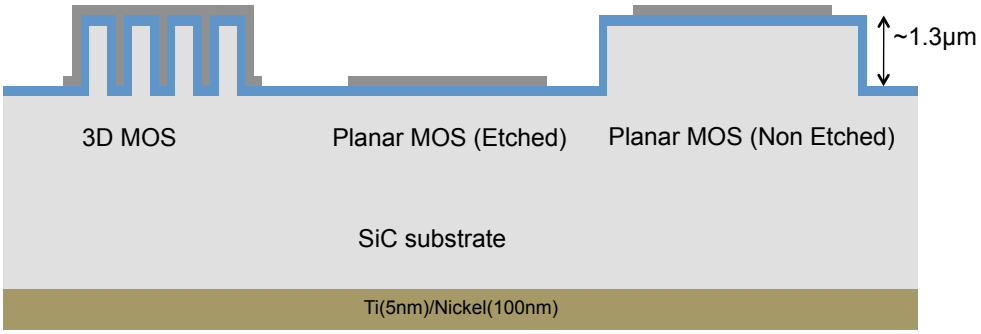


Figure 5.11: Schematic illustration of the cross-section of 3-D gate structure MOS capacitor.

A schematic cross-section of the MOS capacitor with 3-D gate structure is shown in Fig 5.11. The height of the gate structures were 1.3 μm and the width of the top finger was varied between 10 and 1 μm whilst the bottom trench is fixed at 5 and 10 μm.

4° off-axis 4H-SiC samples with a 10.6 μm thick epitaxial layer with a nitrogen concentration of 6×10^{15} cm^{-3} were used as the starting material. A SF_6 and O_2 plasma with power of 200 W at a pressure of 30 mTorr was used to etch trenches of depth of 1.3 μm in a reactive ion etching (RIE) process. After the removal of metal mask, the surface was recovered using a sacrificial oxidation process, followed by BHF dip to remove any process related damage prior to the dielectric deposition. 40 nm of Al_2O_3 was deposited by ALD at 200°C using using trimethylaluminum (TMA) and H_2O as precursors. A Ti (5 nm) / Ni (100 nm) stack was deposited on backside of the wafer and annealed for 200 s at 1050°C in forming gas using an RTP process. Aluminium was deposited using PVD to act as the gate metal and patterned to give contacts with dimensions of 200 μm $\times$ 200 μm.

5.2.2 Results and Discussion

The data in Figure 5.12 show SEM images of a typical 3-D MOS capacitor with the top finger having a width of 1 μm, the bottom of the trench of 5 μm with a height difference of 1.3 μm.

As can be observed in the image, the 3-D structures were fabricated with an excellent trench profile that shows no evidence of fencing or trenching at the foot of the sidewalls.

The data in Fig 5.13 show the C-V and G-V characteristics of the 3-D MOS capacitor structures with different sidewall areas. The data is plotted as a function of gate overdrive $(V_G - V_{\rm FB})$ based on the flatband voltage extracted for the planar structures. In the legend, T refers to the width of the finger and B the width of the trench in μm. The capacitance data show an enhancement in the accumulation capacitance, which increases with the sidewall area. The increase in the capacitance as a function of the capacitor surface area is shown by the data in Fig 5.13, with a 43% enhancement observed. The linear relation between the accumulation capacitance and the surface area of the capacitor indicates that the ALD process used for the growth of the Al_2O_3 is conformal, with identical film thicknesses on the sidewalls and (0001) planes. This is in contrast to what is typically observed with thermally grown SiO_2 on SiC, which is significantly thicker on the sidewalls, resulting in a reduction in the capacitance increase with the formation of a 3D structure [132, 235]. The capacitance data in the figure also show what appears to be a second MOS depletion characteristic located at $V_G - V_{\rm FB} \approx 2$ V. Using standard analysis (the difference in capacitance at each step of the gate voltage is proportional to the doping concentration), the dopant concentration related to the two regions can be extracted – giving 6.0×10^{15} cm^{-3} for the lower voltage (at around

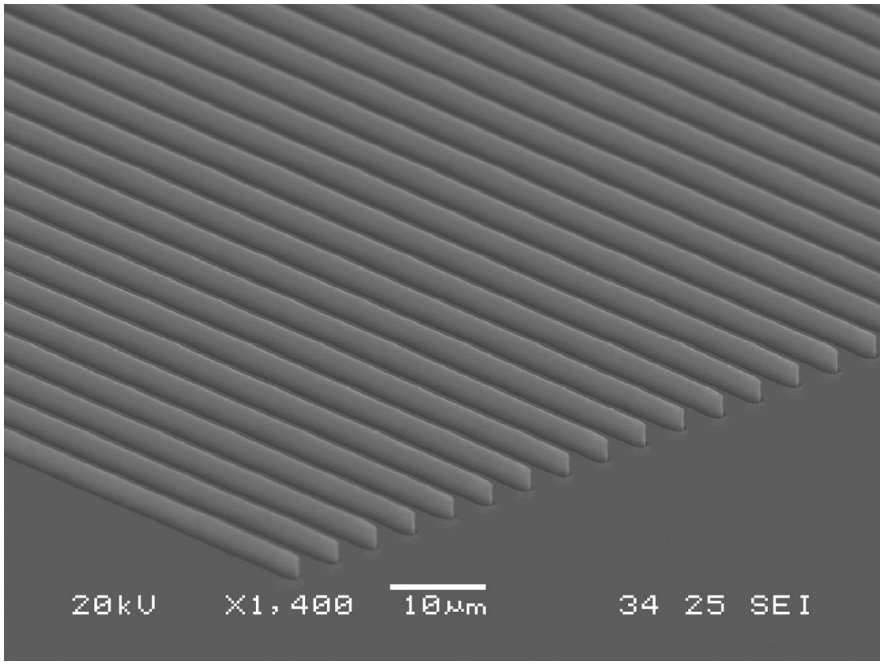


Figure 5.12: SEM images of a typical 3-Dimentional gate structure of 3-D MOS capacitor formed by RIE using Ti/Ni as a mask.

$V_G - V_{\mathrm{FB}} = 0$ V), which is related to the (0001) surface and $1.0{\times}10^{18}$ cm^{-3} for the higher voltage section ($V_G - V_{\mathrm{FB}} \approx 2$ V), which is related to the sidewall. The dopant concentration of the lower voltage matches the dopant concentration in the epilayer used to fabricate the devices, whilst the higher voltage one is significantly higher, as reported previously for SiO_2 based dielectrics on SiC [239].

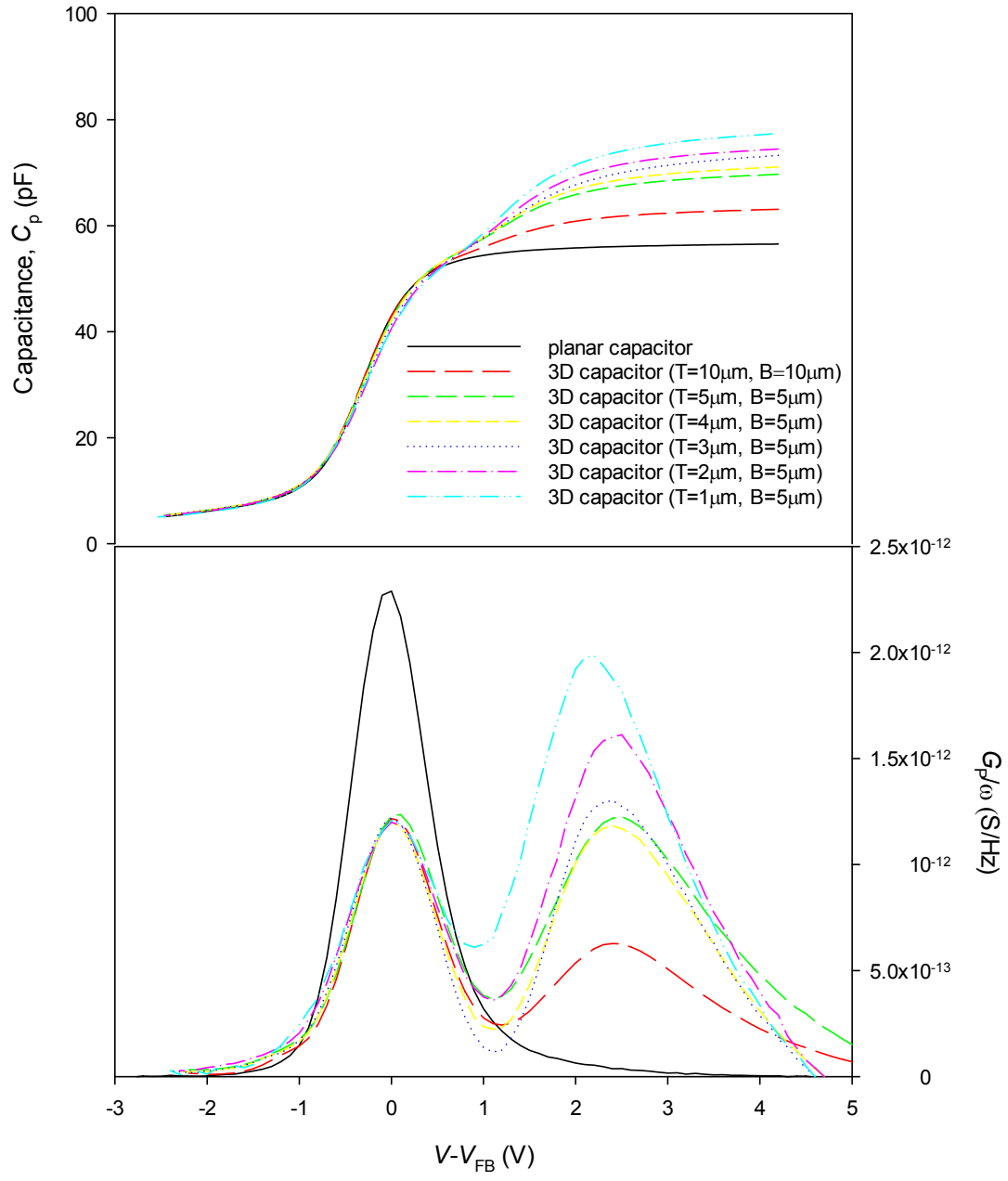


Figure 5.13: 1 MHz C-V and G-V characteristics of 3D MOS capacitors at room temperature.

The data in Fig 5.14 also show the variation in peak conductance for the capacitors. The planar devices show a single conductance peak, located at the flatband voltage that is fully symmetric, suggesting that the dielectric / SiC interface is of high quality. The 3D structures that showed

evidence of the second capacitor in the characteristics also show a second conductance peak that is located at $(V_G - V_{\mathrm{FB}}) \approx 2.5$ V. The influence of the sidewall angle on the additional capacitance and conductance characteristics observed in the data from Fig 5.13 was also studied in this work. However, there is no significant difference observed in terms of either the accumulation capacitance or the height of the conductance peak with changes in the angle. One possible explanation for the lack of a significant difference in the characteristics is related to the tilt angle of the trench sidewalls from the actual crystal plane since the 3-D MOS capacitors were fabricated on a commercial 4° off wafer [240]. Reduction of the offcut angle may yield a greater level of clarity in this regard, however the data presented here is relevant to the realisation of devices on commercially available production grade wafers. For the data reported here, for one 3-D structure, the data includes contributions from two planes of $(11\bar{2}0)$ and $(\bar{1}\bar{1}20)$ on the same structure. It was reported that the mobility of $(\bar{1}\bar{1}20)$ is only half that of $(11\bar{2}0)$, which is the opposite plane[240]. The magnitude of the second peak height scales with the surface area of the sidewalls, as shown by the data in Fig 5.13. The different heights of the peaks in the conductance – voltage characteristics are related to the capacitance of the traps at the SiC/SiO_2 interface and the trap generation / recombination time constant. The conductance, G_{P}, normalised by the angular frequency of the exciting voltage can be expressed as

$$\frac{G_{\mathrm{P}}}{\omega} = \frac{C_{\mathrm{it}}}{2\omega\tau_{\mathrm{p}}} \ln\left[1 + (\omega\tau_{\mathrm{p}})^2\right] \tag{5.3}$$

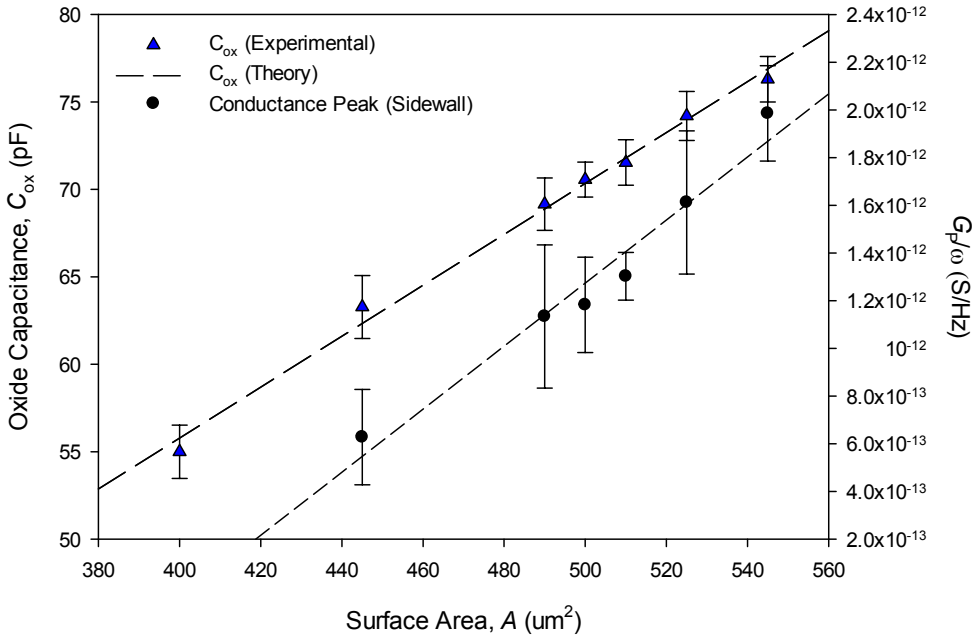


Figure 5.14: Variation in capacitance and conductance with sidewall surface area.

where $C_{\rm it}$ is the capacitance of the interface traps and τ_p the lifetime of the trapping state.

In order to identify the influence of $C_{\rm it}$ on the peak height, the distribution of interface state density as a function of energy for the 3D capacitor structures with different sidewall areas is shown by the data in Fig 5.15. The interface state density was extracted from quasi static capacitance measurements using the $C-\psi$ technique, which accurately measures the concentration of interface state density including fast trap (respond to higher than 1 MHz) at the dielectric interface [121]. The unetched planar capacitors that were fabricated alongside the 3D structures show the expected exponential dependence of $D_{\rm it}$ with energy, with a value of 1×10^{12} cm^{-2}eV^{-1} at $(E_C-E)=0.2$ eV, which is comparable to data published in the literature for a range of dielectrics on 4H-SiC [45, 76]. The etched planar MOS capacitors exhibit a slight increase in the interface state density near the conduction band [239]. As can be seen from the data in the figure, the value of $D_{\rm it}$ close to the conduction band increased with the sidewall area. The legend for each capacitor describes the width of the finger (T value) and the width of the trench (B value). The data in Fig 5.16 show a linear relation between the area of the sidewall and the interface state density that has been extracted from the $C-\psi$ technique

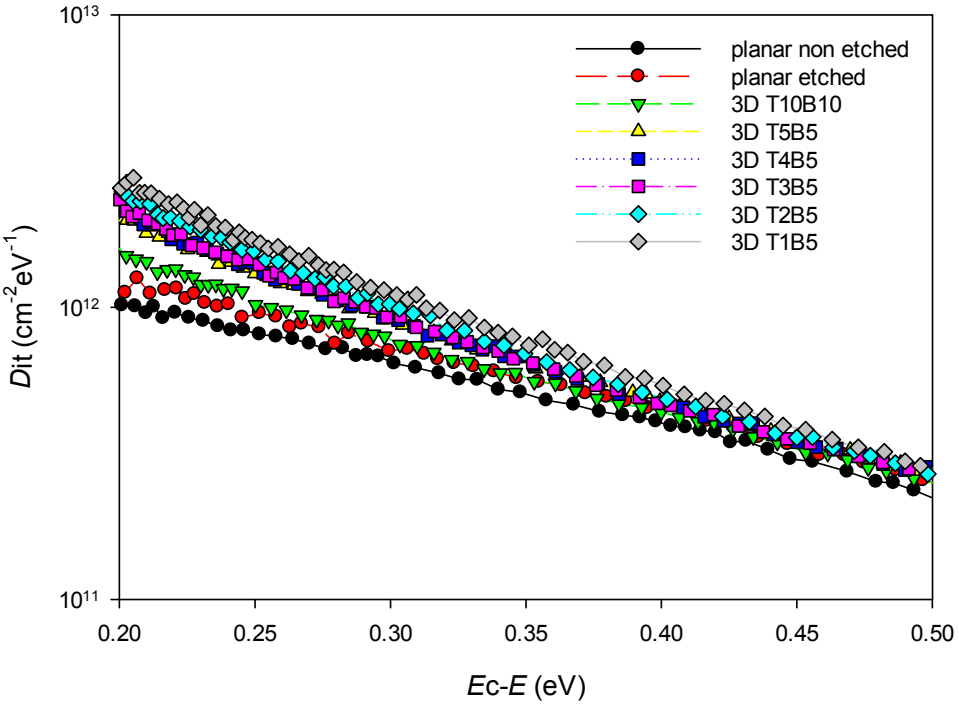


Figure 5.15: The distribution of interface state density as a function of energy within the bandgap, extracted using the $C-\psi$ technique for 3D MOS capacitors with different sizes. Planar capacitors of etched and non-etched were also included in the figure as a reference.

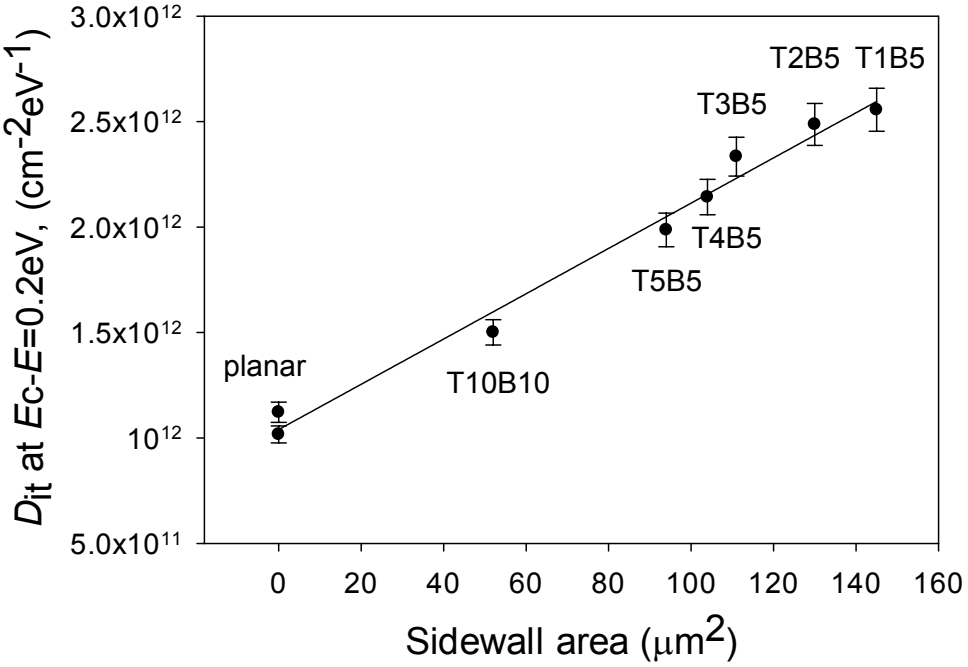


Figure 5.16: Interface state density of 3-D MOS capacitors near conduction band, $E_c - E$=0.2 eV as a function of sidewall area, extracted using $C - \psi$ technique.

close to the conduction band. The two data points at zero sidewall area relate to the unetched surface (lower point) and the etched surface (upper point) confirming that the additional surface roughness does not play a significant role in the interface state density values reported. The data show a factor of 3 increase in $D_{\rm it}$ for the T1B5 structure in comparison to the T5B5, which correlates with the increase in conductance peak height seen in Fig 5.13. Hence, the difference in the conductance peak height with changes in the capacitance is thought to arise from trapping states at the SiC/SiO_2 interface, rather than changes in the recombination / generation lifetime.

These results are in good agreement with those published for FinFET structures in other materials, including silicon and InGaAs [241, 242] where the interface state density at the sidewall is high in comparison to that at the top surface. In silicon FinFET technology, the surface damage and sidewall profile have became issues for the electrical characteristics. In order to improve the surface of the trench structure on the sidewall, previous reports in the literature state that hydrogen annealing is effective in reducing surface roughness and hence improve the electrical characteristics such as gate leakage, subthreshold slope and drain-induced barrier lowering in SiC [243].

The origin of the higher flatband voltage for the sidewall component of the characteristics can be described by the difference in the polar nature of the two different surfaces. The observed

shift in the flatband voltage for the two conductance peaks cannot be explained by the observed shift in the position of the Fermi level that arises from the different dopant concentrations extracted from the capacitance – voltage characteristics. The Fermi level will rise by 0.125 V, which is an order of magnitude lower than the 2 V shift observed in the conductance data. The effect of different crystallographic surfaces on the characteristics of polar semiconductors has been described previously [244] and the increased voltage is related to the higher density of unsatisfied chemical bonds that are formed on the sidewall of the 3D structure.

The existence of the non-ideal features in the positive capacitance and conductance characteristics of the 3D structures will not degrade the behaviour of the transistor when operated in a circuit. When operating in the on-state, the bias on the capacitor is such that the surface of the semiconductor is inverted, forming the conductive channel. For the data presented here, this equates to the application of a negative bias where the characteristics of the 3D structure are identical to those of the planar devices.

The data in Figure 5.17 show the leakage current density through the Al_2O_3/SiC junction. The data show the critical electric fields of 3.4 MVcm^{-1} for the planar and 3.2 MVcm^{-1} for the 3D structures. These values are comparable to the 4 to 5 MVcm^{-1} reported in the literature for amorphous Al_2O_3 on Si [205], which indicates that the high temperature annealing does not result in the formation of an underlying SiO_2 layer. The breakdown field for the 3D structure is lower than for the planar device, suggesting that the inclusion of the sidewall reduces the oxide quality but the conduction band offset is unchanged, indicating that the sidewalls do not have a significantly higher surface charge density than the planar (0001) surface. This supports the hypothesis that the increase in D_{it} for the 3D structures is related to the high density of unsatisfied chemical bonds at the surface of the sidewall. However, the breakdown field for both the planar and 3D structures remains above 3 MVcm^{-1}, which is sufficient to form an inversion layer and hence operate the transistor.

5.2.3 Summary

The data show that 3-D gate structures (Fin MOS) capacitors, a key component of nanoscale MOSFETs, hold the promise of achieving high capacitance densities on the same footprint area, with a demonstrated enhancement of 43%. The enhancement of the accumulation capacitance is linearly dependent on the sidewall area of the capacitor. The capacitance–voltage characteristics for the 3D structures show evidence of a second depletion behaviour at a higher

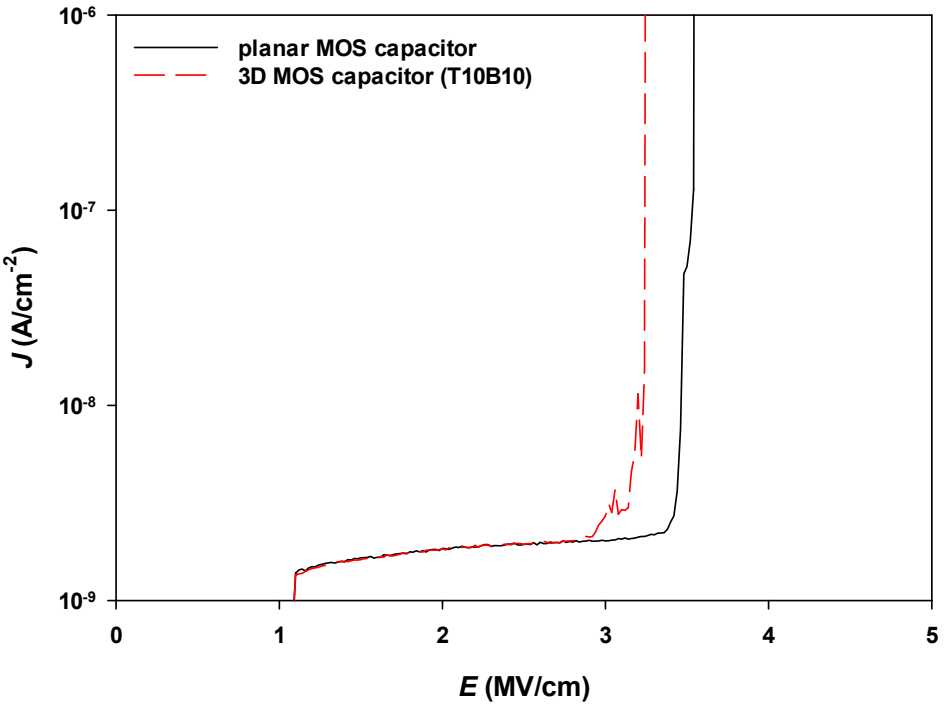


Figure 5.17: Leakage current density through the Al_2O_3 film, for both planar and 3D structures.

flatband voltage than those observed in a purely planar device and this second flatband voltage is identical to the location of a second peak in the G/ω–V characteristics. The chemistry of any unterminated chemical bonds on the sidewall is different to that of the planar (0001) surface and this results in the observed second flatband voltage in both the C–V and G/ω–V characteristics, as well as the observed increase in the interface state density, D_{it}. This work shows that the 3D structure is highly promising for the fabrication of high temperature logic devices for extreme environments.

5.3 Analysis of 3-Dimensional 4H-SiC MOS capacitors grown by atomic layer deposition of Al_2O_3 at high temperatures

1 MHz C-V measurements were performed at temperatures up to 300°C. The data in Figure 5.18 show the change in accumulation capacitance as a function of temperature for 3-D-MOS capacitors with planar MOS capacitors as a reference. As can be seen from the data, the accumulation capacitance of the capacitors (planar and 3-D MOS) increases almost linearly with temperature, indicating that the properties of the Al_2O_3 dielectric layer have a temperature dependence [245–247]. This observation suggests that the origin of this behaviour is the Al_2O_3

dielectric layer because it occurs in both planar and trenched structures. Besides, this might also be due to the temperature dependence of dielectric constant, κ that is proportional to the oxide capacitance, in this case κ value changes from 6.5 to 8 with temperature [248]. The data in Figure 5.19 show the change in flatband voltage as a function of temperature for both planar and 3-D capacitors. The data indicate that the change in flatband voltage between forward and reverse bias sweeps increases with temperature. In general, the change of the flatband voltage reduces for 3-D MOS capacitor with larger sidewall surface area. We conclude that this is due to the incorporation of a surface orientation in the sidewall (including the $(11\bar{2}0)$ orientation), where the flatband voltage was reported to have a lower temperature dependence in comparison to the conventional planar (0001) surface, in agreement with [235].

5.4 Effect of post oxidation annealing (POA) on the 3D MOS capacitor

5.4.1 Effect of post-oxide annealing on the electrical and interface 4H-SiC/SiO_2 3D MOS capacitors

The effect of post-oxide annealing (POA) using nitrogen gas (N_2) at 1000°C for 10 minutes and forming gas (5% H_2 in N_2) at 1150°C for 200 s on 3-D 4H-SiC metal-oxide-semiconductor with different trench sizes and sidewall planes was investigated. These temperatures are selected because they can be used for the formation of back contact. It is assumed that no oxidation process took place during POA and the thickness of SiO_2 remained the same. For the combined treatment sample (N_2 + forming gas), the samples underwent the POA process first and then were annealed in forming gas during the formation of the nickel silicide back contact. The data in Fig 5.20 show the effect of annealing in N_2 gas and combined (N_2 + forming gas) on the C-V characteristics of the 3-D MOS capacitors measured at 1 MHz at room temperature with as-deposited sample as a reference. The gate voltage was swept from accumulation to depletion and vice-versa. All samples demonstrate a small hysteresis (clock-wise), indicating the small amount of the slow traps in the gate oxide. In comparison to the as-deposited sample, the C-V curves of the samples that have been annealed are shifted in the negative direction, resulting in a lower flatband voltage which is within 0.1 V of the ideal flatband voltage. The C-V curves for the samples annealed in (N_2) and combined gas (N_2 + forming gas) overlie, indicating that the process during the formation of back contact after POA of the gate dielectric did not affect the C-V characteristics. Both annealing processes also reduce the amplitude of the defect related bump visible near the flatband which originates from interface states that

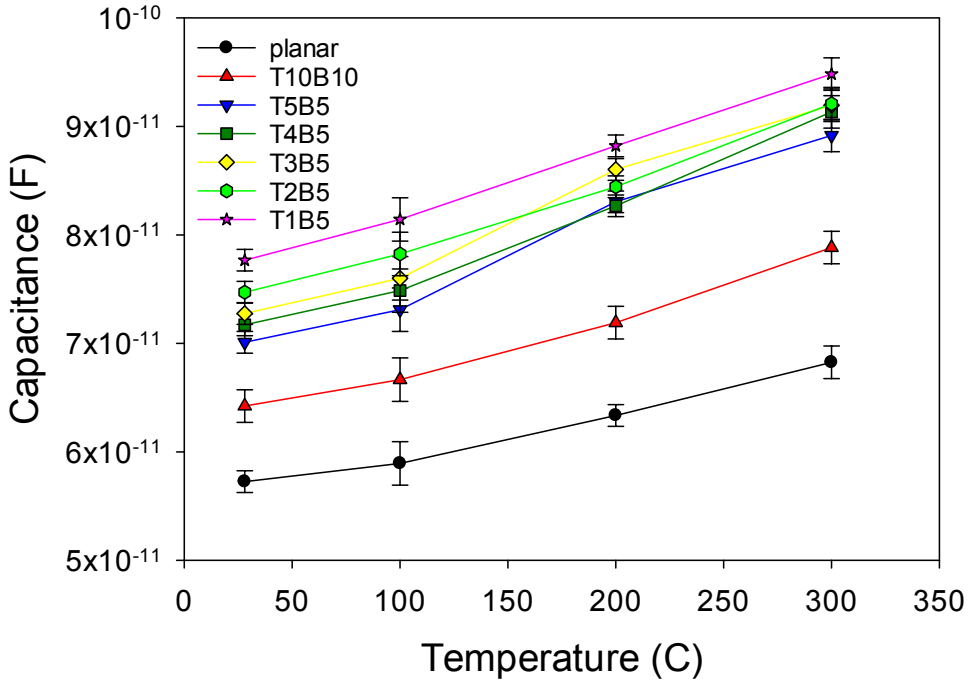


Figure 5.18: Change in oxide capacitance from 1 MHz C-V characteristics as a function of temperature for 3-D MOS capacitors showing samples with different trench sizes.

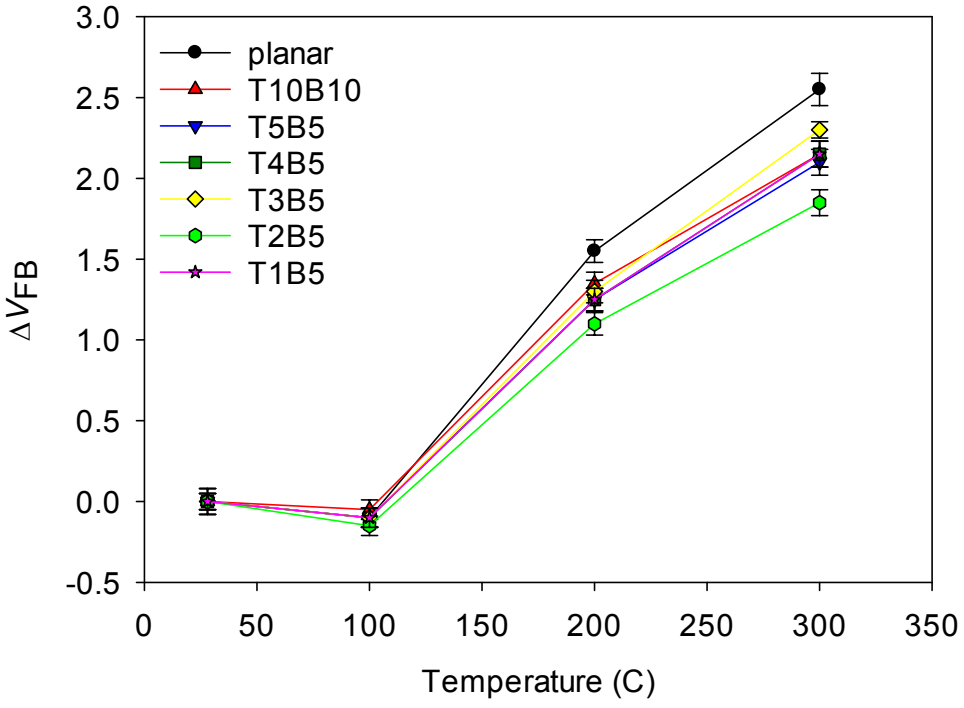


Figure 5.19: Change in flatband voltage from 1 MHz C-V characteristics as a function of temperature for 3-D MOS capacitors.

appear in the conductance signal at different voltages for the as-deposited sample as shown in Fig 5.21. The interface state density of the samples extracted using the Terman method are

shown in Fig 5.22. The data in Fig 5.22 show that annealing process at 1000°C has succesfully reduced $D_{\rm it}$ by approximately one order magnitude in comparison to the as deposited sample. It is well known that H_2 or forming gas annealing has limited effect in reducing $D_{\rm it}$ [4] because H_2 has a large diffusion barrier in SiO_2 and requires a relatively high temperature. However, the result of combined gas annealing shows that there is a noticable decrease in $D_{\rm it}$ deeper in the bandgap ($E_c - E \geq$0.4 eV) and this is in a good agreement with previously reports [66].

5.4.2 Effect of post-oxide annealing on the electrical and interface of 4H-SiC/Al_2O_3 3D MOS capacitors

This section reports on the effect of forming gas annealing on the C-V characteristics and stability of Al_2O_3/SiC MOS capacitors deposited by atomic layer deposition (ALD). C-V and I-V measurements were performed to assess the quality of the Al_2O_3 layer and the Al_2O_3/SiC interface. The results provide an indication the possibility to improve the performance of Al_2O_3/SiC capacitors 4H-SiC devices by optimizing the annealing temperature.

The need for highly reliable dielectric films for SiC devices has become increasingly urgent to enable their deployment in hostile environments, such as those found in aerospace and oil and gas exploration. SiO_2 is the most popular gate dielectric owing to its superlative material properties [98]. However, SiO_2 has limitations for devices that operate at high temperatures or with high electric fields [59]. The static dielectric constant of SiO_2 (3.9), which is low in comparison to that of SiC, results in a high electric field in the SiO_2 for devices operating at high voltages. Therefore, a new highly reliable dielectric with permittivity similar to that of SiC is required. A range of dielectrics including hafnium dioxide (HfO_2), aluminium oxide (Al_2O_3) and lanthanum oxide (La_2O_3) have been investigated in terms of performance and reliability [100]. Al_2O_3 is a potential high-κ material with conduction and valence band offsets of 1.7 eV and 1.2 eV respectively, sufficient to prevent electron and hole injection [101]. The band offset can be further increased by the deposition of a thin layer of SiO_2 before Al_2O_3 deposition [102].

High channel mobility in 4H-SiC MOSFETs with Al_2O_3 gate dielectric has been previously demonstrated [86]. The interfacial properties of Al_2O_3/ SiO_2/ SiC was reported to be better than Al_2O_3/ SiC in terms of leakage current and interface state density, $D_{\rm it}$ [96]. It has been reported that post-oxide annealing (POA) of Al_2O_3 in H_2 at 500°C reduced $D_{\rm it}$ to the level of 10^{11} cm^{-2} eV^{-1} in the mid-gap of 6H-SiC. However, due to significant charge trapping

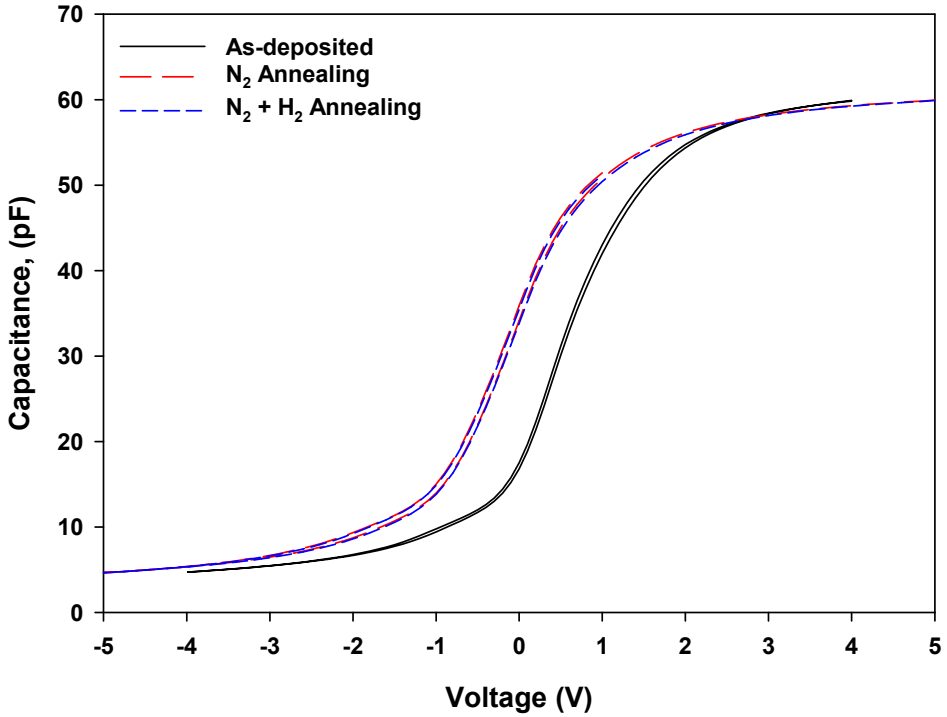


Figure 5.20: C-V characteristic of 3-D MOS capacitors with different annealing.

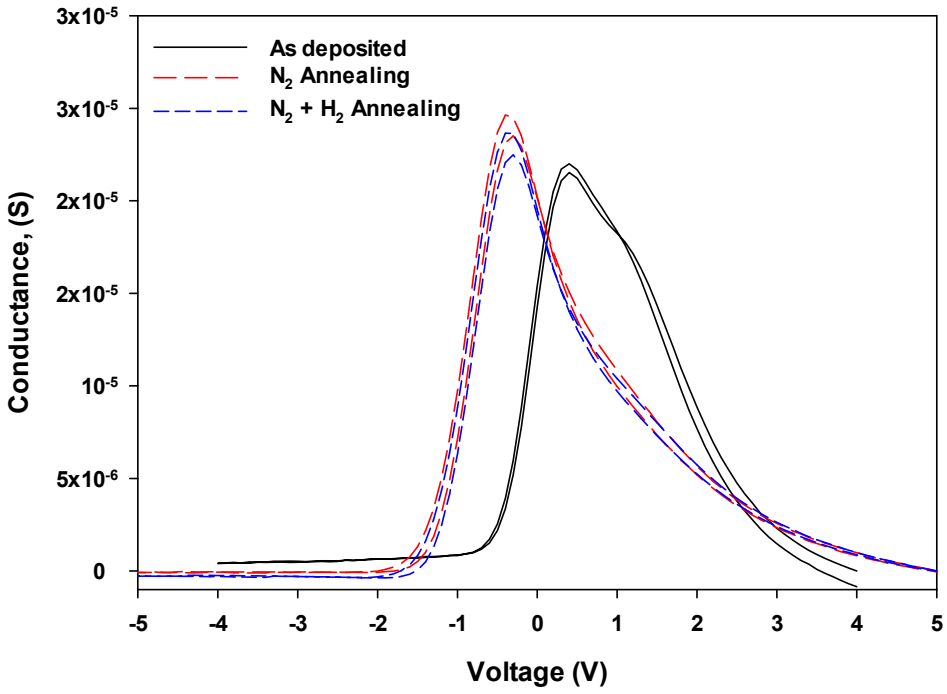


Figure 5.21: G-V characteristic of 3-D MOS capacitors with different annealing.

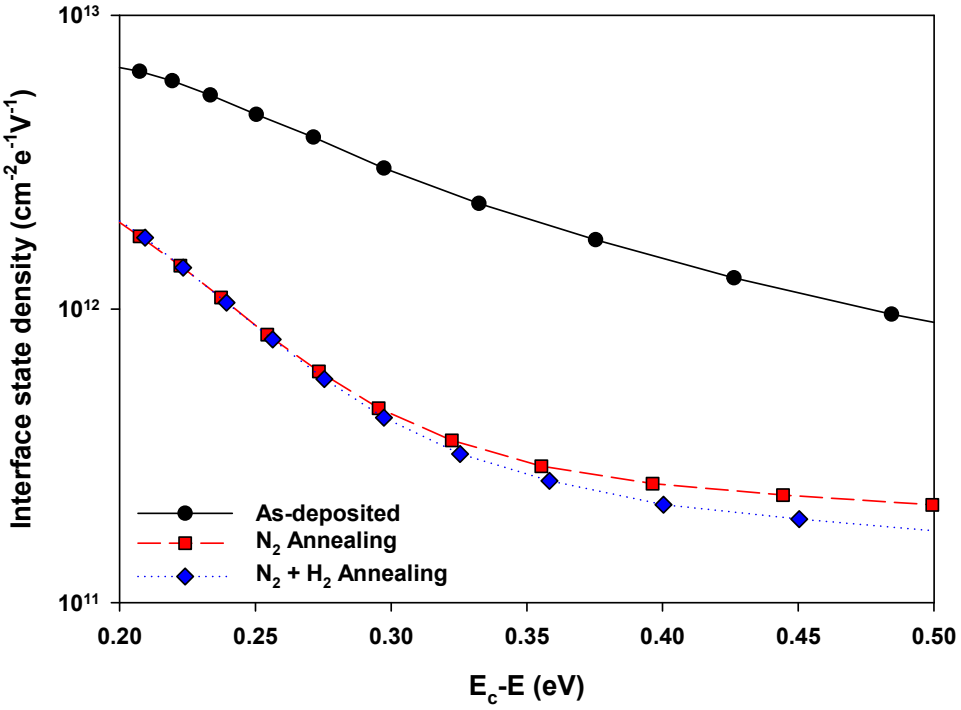


Figure 5.22: Interface state density of 3-D MOS capacitors with different annealing.

phenomena in the oxide and at the interfaces, significant hysteresis in the C-V characteristics and deviation in flatband voltage with different bias voltages were observed [96, 104]. More recently reports indicate that post deposition hydrogen treatment is a promising technique for the reduction of $D_{\rm it}$ at the 4H-SiC / Al_2O_3 interface; however the stability of C-V characteristics remains to be determined. Hence, this work reports the first systematic study on the effect of annealing temperature in a hydrogen rich ambient on 4H-SiC/ Al_2O_3 MOS capacitors.

5.4.3 Experimental

N-type 4H-SiC, 4° off axis epilayers with a nitrogen concentration of 5.8×10^{15} cm^{-3} were used in this experiment. First, the samples were cleaned using solvents, then treated with piranha solution prior to standard RCA cleaning followed by sacrificial oxidation at 1150°C for 1 hour. 40 nm of amorphous Al_2O_3 was deposited on HF dipped 4H-SiC samples by means of atomic layer deposition at a substrate temperature of 200°C. Trimethylaluminum (TMA) and H_2O were used as precursor and oxygen source respectively. H_2 gas carrier was used for the purging process. The samples were subjected to post-oxide annealing at 450°C and 1050°C

in forming gas (5% of H_2 diluted in N_2). Aluminium was evaporated for the gate metal. For the formation of the back contact, titanium (5nm) / nickel (100nm) were deposited on the highly doped back side of the samples and annealed at 1050°C for 200 s in forming gas.

5.4.4 Result and Discussion

Electrical characteristics of the MOS capacitors after annealing at different temperatures (as-deposited, 450°C and 1050°C using a rapid thermal annealing) were investigated. The hysteresis data in Figure 5.23 (left) show that the stability of the C-V curves and flatband voltage were significantly improved after annealing at 1050°C. From the data in Figure 5.23 (right), it can be seen that the oxide capacitance drops with increasing annealing temperature with the data point for 1050°C showing a reduction of approximately 20% in comparison to the as deposited sample. This decrease in capacitance may be due to changes in the bulk permittivity of the Al_2O_3 or the formation of a thin (4.5 nm) SiO_2 layer at the Al_2O_3/SiC interface. The oxygen required to form this layer would originate from residual oxygen from the amorphous Al_2O_3 depostion [249].

The data in Figure 5.23 show the hysteresis extracted from C-V curves for samples annealed at different temperatures. C-V measurements were performed from accumulation to depletion and vice-versa to determine the hysteresis. The as-deposited samples show large hysteresis in the C-V characteristics of approximately 2 V. The hysteresis of the C-V curves reduces with annealing temperature with the samples annealed at 1050°C exhibiting a hysteresis of 0.2 V, indicating a significant reduction in mobile charged defects, often ascribed to oxygen vacancies or carbon impurities in the Al_2O_3 film [250].

To further investigate the stability of the C-V characteristics, the measurements were repeated 3 times on fresh capacitors. The data in Figure 5.24 show that the C-V curves shift to more positive bias for repeated measurements in comparison to the as-deposited samples. The magnitude of the shift reduces with increasing annealing temperature, with a minor variation observed in the samples annealed at 1050°C. This indicates that the effect of negatively charged defects can be reduced by increasing the temperature of the post-oxide anneal.

The stability of the flatband voltage for different start voltages (the voltage at which the voltage sweep starts during the C-V measurement) was also investigated. To obtain more insight into the previous data, the C-V measurements were also collected with starting voltages of 5, 7 and 10 V and stop at -5 V. The data in Figure 5.25 show that the stability of flatband voltage with

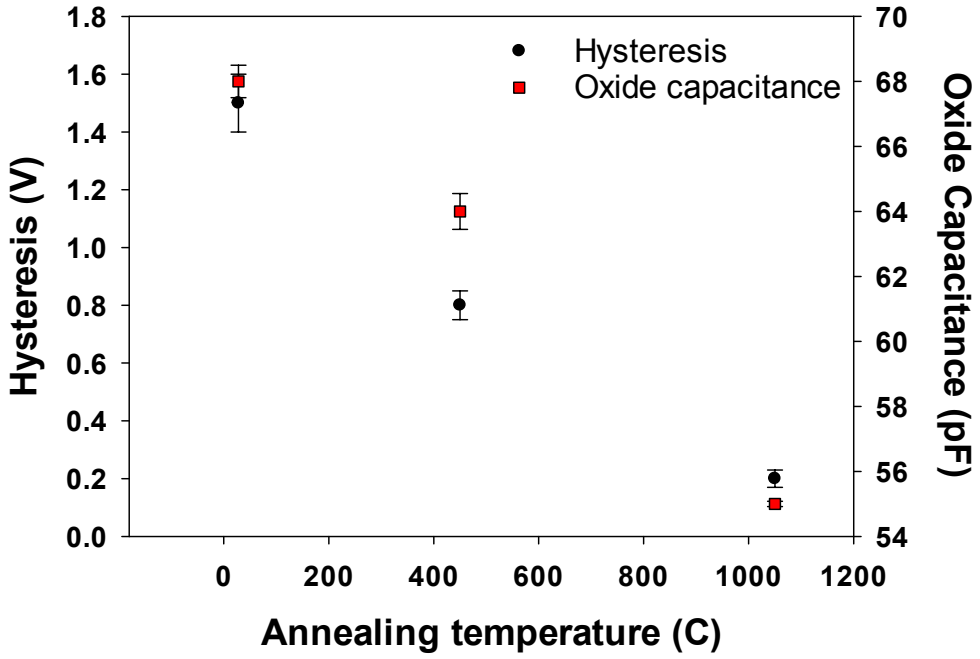


Figure 5.23: Hysteresis of samples with different annealing temperatures. Change in oxide capacitance of samples with different annealing temperatures.

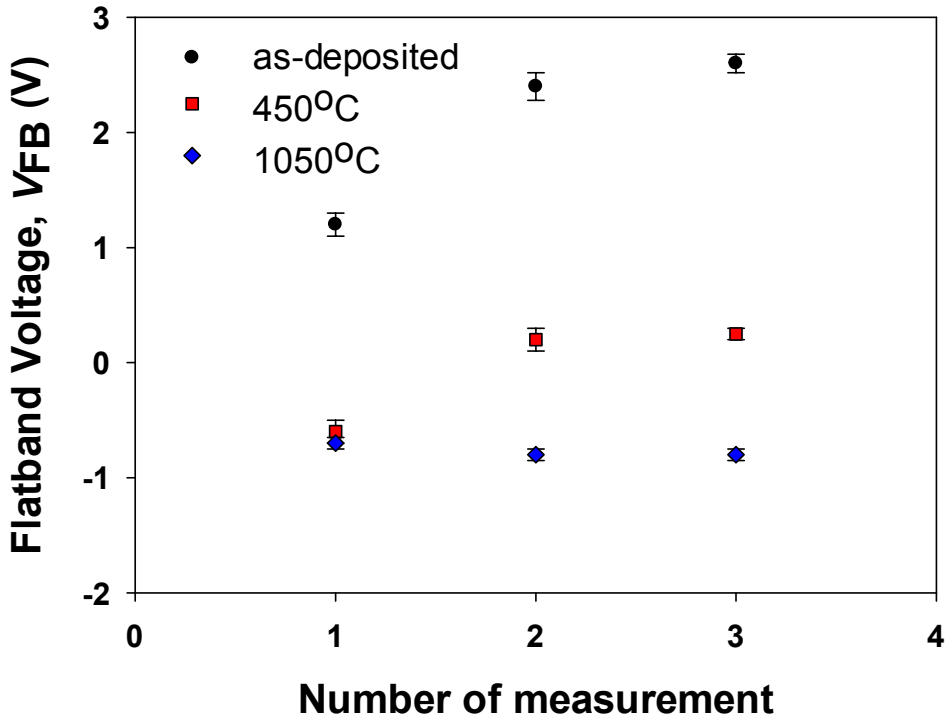


Figure 5.24: Change in flatband voltage, V_{FB} for samples as a function of the number of measurements. The measurements were repeated on the same samples.

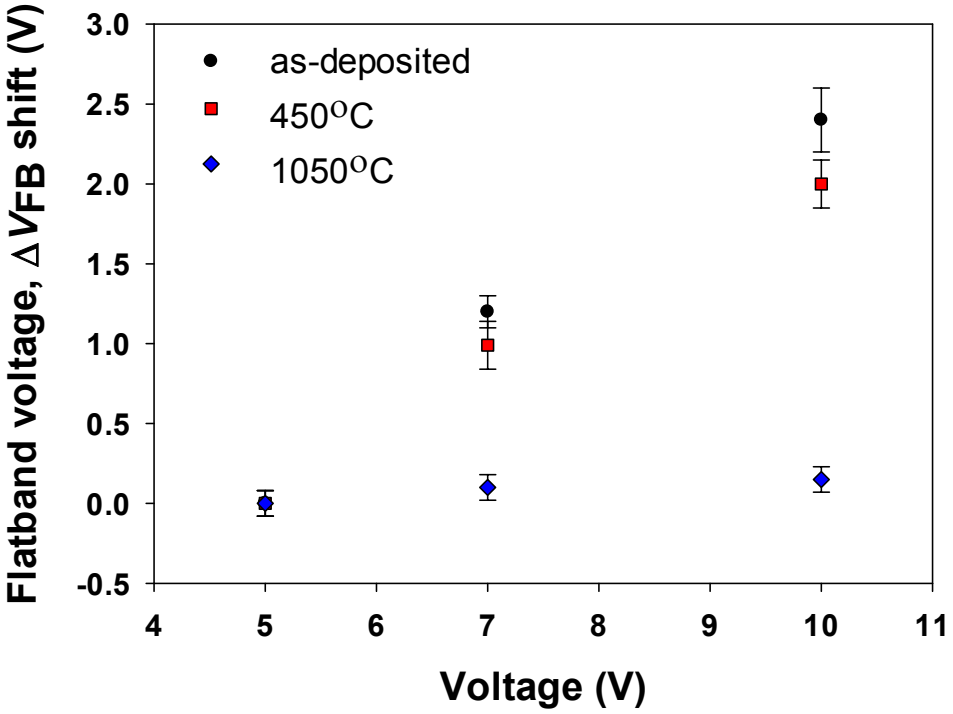


Figure 5.25: V_{FB} shift as a function of the starting voltage. Gate voltage of 5, 7 and 10 V were applied from the accumulation region to depletion region.

different applied voltages improves with increasing annealing temperature. The C-V curves were shifted to the negative, indicating that the magnitude of negative charge in the oxide has reduced. The data for the capacitors annealed at 1050°C indicates that it is possible to form Ohmic contacts after the deposition of the high-κ film, offering a simpler fabrication process for a MOSFET, because 1050°C is used in ohmic contact formation [249].

The density of interface traps, $D_{\rm it}$ was extracted using the $C - \psi_s$ technique and the data are shown in Figure 5.26. The data show that annealing reduces $D_{\rm it}$ close to the conduction band, offering the opportunity for significant improvements in the field mobility in MOSFET structures.

To examine the effect of POA on the leakage current and oxide breakdown voltage, current -voltage (I-V) measurements were performed in accumulation region at room temperature. The data in Figure 5.27 show the J-E characteristics of the samples annealed at different temperatures. From the data in Figure 5.27, it is clear that the sample annealed at 1050°C exhibits the lowest breakdown field of 3 MV/cm in comparison to 5.5 and 7.3 MV/cm for unannealed and annealed at 450°C samples respectively. This trend is expected considering that the crystallization temperature of Al_2O_3 is approximately 1000°C [9] and the likely formation

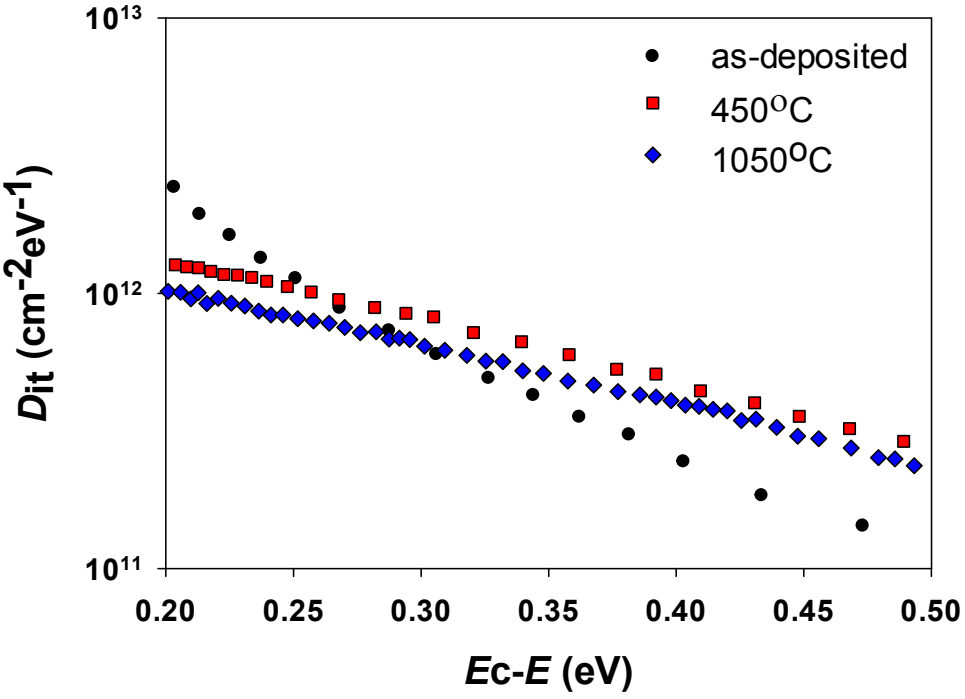


Figure 5.26: Interface trap density, $D_{\rm it}$ as a function of energy at room temperatue. C-ψ technique was used to extract the interface trap density, $D_{\rm it}$.

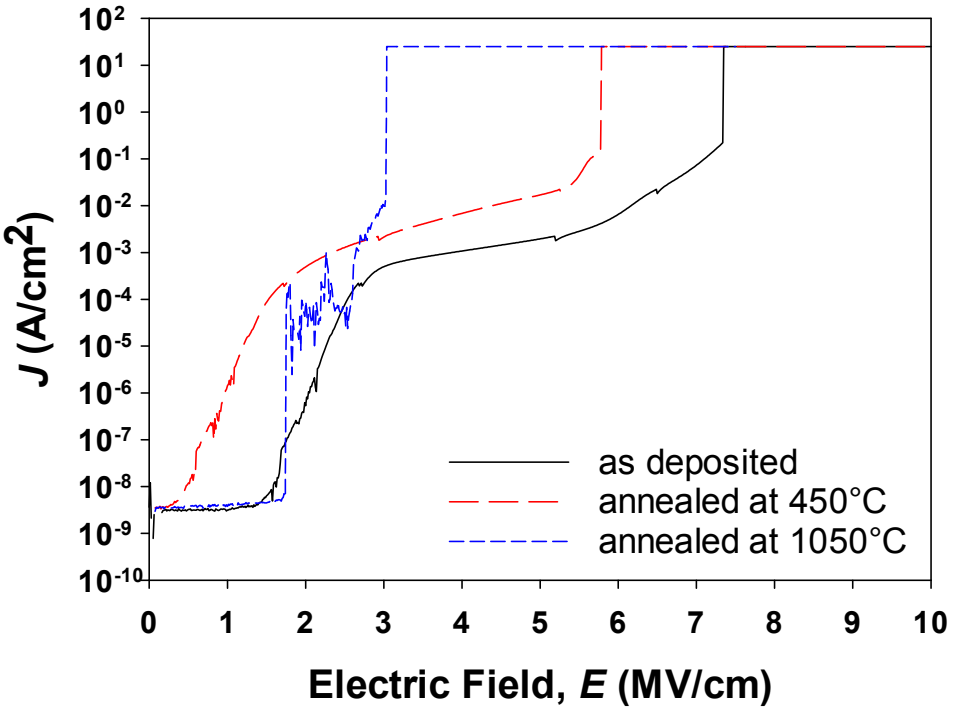


Figure 5.27: Current density- Electric field (J-E) characteristic of Al_2O_3/SiC MOS capacitors annealed at different temperatures.

of an interfacial layer at the Al_2O_3/SiC interface, which is not effective for the supression of the leakage current [84, 249]. Although it has been previously reported that POA has improved the insulating properties of Al_2O_3 ALD film on silicon [210], in this work, the insulating properties of Al_2O_3 layer in term of leakage current and oxide breakdown degrade with the increasing anneling temperatures even at moderate temperature of 450°C indicating that the Al_2O_3 crystallisation initiates around temperature. The results presented excellent agreement with work published elsewhere [107].

5.5 Conclusion

3-Dimensional MOS capacitors were realized by plasma enhanced chemical vapour deposition (PECVD) of SiO_2, yielding an enhanced oxide capacitance, C_{OX} which scales with increasing surface area. The analysis of the oxide capacitance enables the determination of the thickness of oxide on the sidewall to be around 20 nm. In comparison to the planar MOS capacitor, the interface state density of the 3-D MOS capacitors increased with the number of trenches due to the surface damage on the sidewall during the etching process by RIE. The effect of nitrogen and hydrogen incorporation into SiO_2/SiC interface are studied on device characteristics including the flatband voltage, effective oxide charge and interface state density. Post-oxide annealing in nitrogen environtment significantly reduces the interface state density in entire energy range for PECVD SiO_2.

The 3-D MOS capacitors demonstrate higher accumulation capacitance in comparison to planar MOS capacitors. Atomic layer deposition is a very promising technique for depositing gate dielectric for the 3-D structure MOS capacitors due to its properties for providing conformal coverage of high aspect ratio structures. Nevertheless, the data show that D_{it} increased with the sidewall surface area. Despite the increase in the density of interface traps on the sidewalls, the development of 3-D structures in SiC offers significant promise for the realisation of high-performance MOSFET devices in the future. In addition, the 3-D MOS capacitor also has a different temperature dependence of flatband voltage in comparison to conventional planar MOS

The use of POA in hydrogen rich ambient is a suitable route to the realisation of high performance MOSFET structures and enables flexibility in terms of the process flow and overall thermal budget. Hydrogen passivation by annealing in forming gas, which has been previously considered to be ineffective has shown good results for Al_2O_3/SiC MOS characteristics.

Formation of thin layer SiO_2 at the interface can be taken into account for the reduction of oxide capacitance of Al_2O_3/SiC MOS capacitors after annealed at 1050°C. Nevertheless, the data shows that although the annealing process at 1050°C improves the electrical and interface characteristics of Al_2O_3/SiC, the reliability properties of Al_2O_3 in terms of leakage current and oxide breakdown voltage degrade, most likely due to the crystallization of Al_2O_3 layer approximately at 1000°C. The finding results suggest that the optimization of POA in hydrogen gas between 500°C to 1050°C is the key to improving the electrical and interface characteristics of Al_2O_3/SiC.

Chapter 6

Conclusions and future work

6.1 Summary

This thesis focused on the issues related to SiC interface based on MOS and MOSFET devices including interface state density, flatband voltage, threshold voltage and field effect mobility. As presented in chapter 2, SiC technology with excellent materials properties offers superlative solutions, especially in extreme environments where silicon technology has reached the limit. Although SiC devices are now commercially available, there is still plenty pf room for improvement to fully utilise the advantages of the material properties for electronic applications. One of the crucial challenges for 4H-SiC MOSFETs is to increase the field effect mobility in the channel, which is plagued by the high interface trap density. Post oxide annealing in nitrogen gas environment or nitridation have become standard processes for the fabrication of MOSFETs with acceptable channel mobility, typically around 35 $\mathrm{cm}^2V^{-1}s^{-1}$, only about 4 $\%$ of bulk mobility. POA using phosphorus gas such as $POCl_3$ or P_2O_5 converts SiO_2 into phospho-silicate glass (PSG) and has succesfully improved the channel mobility by a factor of 3 in comparison to nitridation. However, PSG is a polar material that induces instability to MOS devices characteristics especially at high temperatures. In chapter 3, the effect of phosphorus inclusion on SiO_2 was investigated by electrical measurements on MOS capacitors at high temperatures and using different bias stress at high electric fields. The results showed that the incorporation of phosphorus at the SiO_2/SiC interface results in a reduction in the interface state density near the conduction band and an increase in the instability of V_{FB}, V_{TH}, andN_{EFF} at high temperatures. It is also found that the phosphorus increases the instability of the characteristics attributable to the injection of electrons from the semiconductor to the SiO_2. Therefore, the accumulated negative charge in phosphorus-doped SiO_2 due to injection of electrons enhanced by the existence of mobile charge is responsible for the enhanced positive shift in C-V and I-V characteristics.

In chapter 4, the effect of different dielectric formation on the performance of CMOS devices was studied based on the characteristics of MOS capacitors, MOSFETs and inversion MOS capacitors. Important parameters such as interface state density, flatband voltage and

effective oxide thickness extracted from the C-V characteristics of MOS capacitors were used to assess the quality of gate dielectrics at room and elevated temperatures. The results obtained from the MOS capacitors were then compared to the MOSFET characteristics. The results from an n-type MOS capacitor is strongly correlated with n-channel MOSFET, but no correlation was found for p-type MOS and p-channel MOSFET. This suggests that the carrier trapping mechanism at the SiC/SiO_2 interface for n-channel is different with the p-channel, thus resulting in the inconsistant trend. The temperature dependence of MOSFETs parameter including threshold voltage, field effect mobility and subthreshold swing were investigated. The reduction of the band gap and electron detrapping at elevated temperatures are cause the field effect mobility to increase with increasing temperature for both n and p-channel MOSFETs. However, the field effect mobility for p-channel MOSFET saturates at a temperature of approximately 200°C and slightly decreases at higher temperatures due to the high resistance of the p-channel. Finally, the correlation between inversion capacitance from the inversion MOS capacitor and field effect mobility from MOSFETs was investigated. The results show that the inversion MOS capacitor is a reliable test structure to determine the performance of MOSFETs at room and high temperatures.

Chapter 5 involved a study into the performance of 3-Dimensional MOS capacitors formed in n-type 4H-SiC. Since thermal oxidation cannot be used for the formation of the gate dielectric due to anisotropic growth on the different faces, PECVD and ALD were utilized in this work. The investigation involved both electrical and physical characterisation at room and elevated temperatures. The linear enhancement of oxide capacitance with increasing surface area was observed on the 3 structures of both PECVD and ALD MOS capacitor samples with the latter demonstrating conformal coverage with high aspect ratio strucutres. The interface density on the sidewall is high in comparison to the top surface due to the surface damage resulting from the etching process. The chemistry of the surface plane on the sidewall is different to that of the (0001) planar and exhibits a different temperature dependence of the flatband voltage. This work shows that the 3-D gate structure MOS capacitor is a key component of SiC FinFETs and highly promising for high temperature logic devices.

6.2 Future work

The inclusion of phosphorus atoms at SiC/SiO_2 is promising to improve the field effect mobility. However, the stability and realibility at both room and high temperatures are important so that the advantagous effect of phosphorus incorporation is not wasted. The

optimization process for the incorporation of phosphorus is required to improve the stability of flatband voltage while maintaining the performance. For example, reducing the thickness of the PSG interfacial passivation layer has been proven to improve the threshold voltage stability

The effect of different dielectric formation on n and p-channel 4H-SiC MOSFET was investigated. This work has contributed to the understanding of carrier transport and mobility limiting mechanisms associated to SiC/SiO_2 interface. It is very challenging to obtain a process gate dielectric formation that works excellently on both n and p-channel. Until today, there is still a lack of a compehensive study in the literature describing the challenge of optimizing CMOS devices. For instance, low frequency 1/f noise measurement may provide further insight into the role of oxide trapping on mobility. The utilization of high-κ materials, different surface plane such as $(11\bar{2}0)$ plane and $(1\bar{1}00)$ on p-channel are also interesting topics to be studied in the future.

High capacitance density 3D MOS capacitor was demonstrated in comparison to the planar MOS capacitor on the same footprint. This result is very promising for the fabrication of FinFETs. Further investigation on reducing the surface roughness on the sidewall of 3D structure is required to improve the performance of MOS system for FinFETs. H_2 annealing was reported to be effective to round-off the corners of the fin, smooth the surface on the sidewall and hence improve the electrical characteristics including the gate leakage, subthreshold voltage and drain induced barrier lowering.

The fabrication of 3D-MOSFET/ FinFET 4H-SiC is an interesting and promising effort in improving the performance of drain current in 4H-SiC MOSFET. ALD is a favourable technique to deposit conformal gate dielectric on trench or 3D structure due to its capability to deposit an atomic layer with a excellent precision. The impact of high-k material as a gate dielectric is still a hot topic amongst researchers. The utilization of sidewall plane and larger surface area could have significantly exhibit higher mobilities and relevance for future technology.

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